DLC Display Co., Limited

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MODEL No: DLC0177AZOF-1

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Record of Revision

Date	Revision No.	Summary
2010-03-04	1.0	Rev 1.0 was issued

1. Scope

This data sheet is to introduce the specification of DLC0177AZOF-1, passive matrix OLED module. It is composed of an OLED panel, driver IC. The 1.77″ display area contains 160(RGB) x 128 pixels.

2. Application

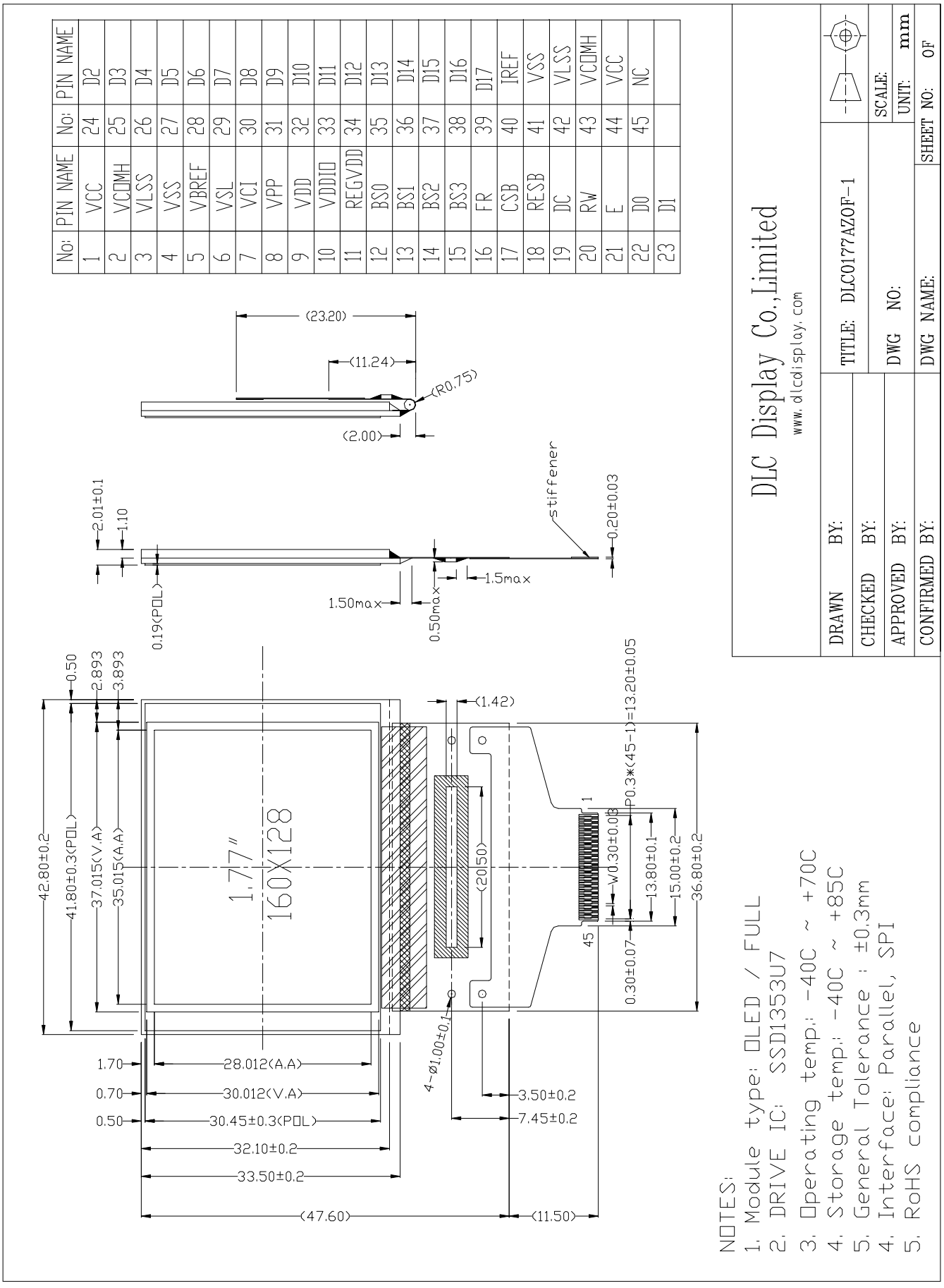
Digital equipments which need color display, mobile phone, mobile navigator/video systems.

3. General Information

Item	Contents	Unit
Size	1.77	inch
Resolution	160(RGB) x 128	/
Display Color	262 K color and 65K colors	
Interface	8/9/16/18-bits 6800/8080-series Parallel Interface, Serial Peripheral Interface	
Pixel size	0.194 (W) x 0.199 (H)	
Pixel pitch	0.219 (W) x 0.219 (H)	mm
Outline Dimension (W x H x D)	42.8 (W) x 33.5(H) x 2.01 (T)	mm
Active Area	35.015 (W) x 28.012 (H)	mm
Driver IC	SSD1353U7	
Operating Temperature	-40℃~+70℃	
Storage Temperature	-40℃~＋85℃	

* Panel thickness includes substrate glass, cover glass and UV glue thickness.

4. Outline Drawing



5. Interface signals

Recommend connector: OMRON XF2B-4545-31A

No	Symbol	Description
1	VCC	Power supply for panel driving voltage.
2	VCOMH	A capacitor should be connected between this pin and VSS.
3	VLSS	Analog system ground pin.
4	VSS	Ground pin.
5	VBREF	Connect to ground with a capacitor.
6	VSL	This is segment voltage reference pin.
7	VCI	Low voltage power supply.
8	VPP	Connect to VDD.
9	VDD	Power supply input for logic.
10	VDDIO	Power supply for interface logic level.It should be match with the MCU interface voltage level. VDDIO must always be equal or lower than VCI.
11	REGVDD	Internal VDD regulator selection pin. When this pin is pulled high,internal VDD regulator is enabled. When this pin is pulled low,external VDD regulator is used.
12	BS0	Interface selection pins.
13	BS1	
14	BS2	
15	BS3	
16	FR	It should be kept NC.
17	CSB	This pad is the chip select input. Low active..
18	RESB	This is a reset signal input. Low active.
19	DC	D/C=”H”: Data. D/C=”L”: Command.T
20	RW	When connected to 8080-series MPU. WR pin.When RW =”L”: Write signal input. When connected to 6800-series MPU. When RW =”H”: Read. When RW =”L”: Write.
21	E	When connected to 8080-series MPU. RD pin.When E =”L”: Read signal input. When connected to 6800-series MPU. Enable clock input of the 6800 series MPU.
22~39	D0~d17	18 bit / 16bit / 9bit / 8 bit Data bus I/O.
40	IREF	A resistor should be connected between this pin and VSS.
41	VSS	Ground pin.
42	VLSS	Analog system ground pin.
43	VCOMH	A capacitor should be connected between this pin and VSS.
44	VCC	Power supply for panel driving voltage.
45	NC	No connection.

6. Absolute maximum Ratings

6.1. Electrical Absolute max. ratings

Parameter	Symbol	MIN	MAX	Unit	Remark
Supply Voltage	VCI	-0.5	3.5	V	
Supply Voltage	VCC	10	21	V	

6.2. Environment Conditions

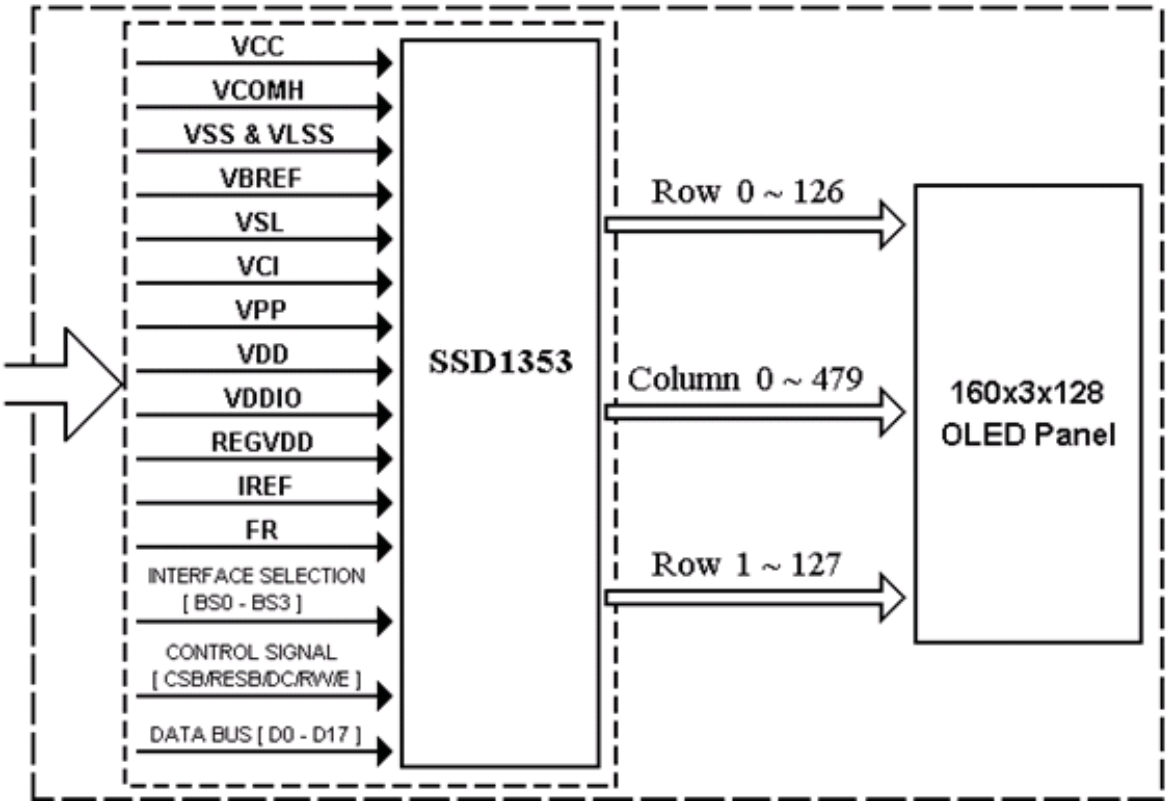
Item	Symbol	MIN	MAX	Unit	Remark
Operating Temperature	TOPR	-40	70	℃	
Storage Temperature	TSTG	-40	85	℃	

7. Electrical Specifications

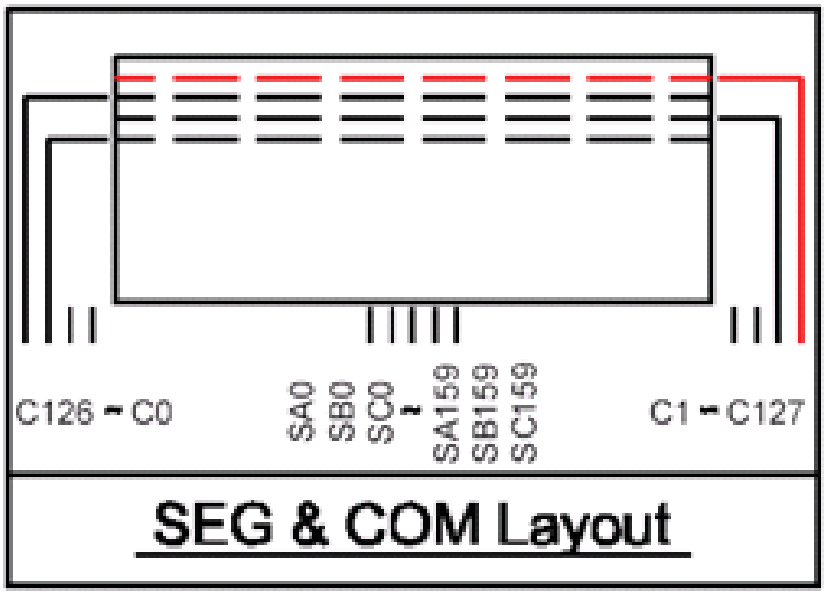
7.1 Electrical characteristics

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Low voltage power supply (for driver IC)	VCI	2.4	2.8	3.5	V	
Logic I/O operating voltage	VDDIO	1.6	1.8	VCI	V	
Driver power supply (for OLED panel)	VCC	16.5	17	17.5	V	
Input Signal Voltage	VIL	0	--	0.2VDDIO	V	Iout=100uA
	VIH	0.8VDDIO	--	VDDIO	V	
output Signal Voltage	VOL	0	-	0.2VDDIO	V	Iout=100uA
	VOH	0.9VDDIO	-	VDDIO	V	
Operating current for VCI (No panel attached)	ICI	--	890	980	uA	Contrast=FF
Operating current for VCC(No panel attached)	Icc	--	8.9	10	mA	Contrast=FF
Segment output current (No panel attached)	ISEG	--	160	175	uA	Contrast=FF
		--	80		uA	Contrast=7F

7.2 FUNCTION BLOCK DIAGRAM



7.3 PANEL LAYOUT DIAGRAM



7.4 GRAPHIC DISPLAY DATA RAM ADDRESS MAP

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 160x132x18bits.For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software.For vertical scrolling of the display, an internal register storing display start line can be set to control the portion of the RAM data to be mapped to the display.Each pixel has 18-bit data. Each sub-pixels for color A, B and C have 6 bits. The arrangement of data pixel in graphic display data RAM is shown below.

Data Format / Common Address		A5	B5	C5	A5	B5	C5	A5	.....	.....	C5	A5	B5	C5	
		A4	B4	C4	A4	B4	C4	A4	.....	.....	C4	A4	B4	C4	
		A3	B3	C3	A3	B3	C3	A3	.....	.....	C3	A3	B3	C3	
		A2	B2	C2	A2	B2	C2	A2	.....	.....	C2	A2	B2	C2	
		A1	B1	C1	A1	B1	C1	A1	.....	.....	C1	A1	B1	C1	
		A0	B0	C0	A0	B0	C0	A0	.....	.....	C0	A0	B0	C0	Common output
Normal	Remapped														
0	131	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM0
1	130	6	6	6					.....	.....					COM1
2	129								.....	.....					COM2
3	128								.....	.....					COM3
4	127								.....	.....					COM4
5	126								.....	.....					COM5
6	125			no of bits in this cell					.....	.....					COM6
7	124								.....	.....					COM7
:	:	:	:	:	:	:	:	:	.....	.....	:	:	:	:	
:	:	:	:	:	:	:	:	:	.....	.....	:	:	:	:	
:	:	:	:	:	:	:	:	:	.....	.....	:	:	:	:	
127	4								.....	.....					
128	3								.....	.....					COM128
129	2								.....	.....					COM129
130	1								.....	.....					COM130
131	0								.....	.....					COM131
SEG output		SA0	SB0	SC0	SA1	SB1	SC1	SA2	.....	.....	SC158	SA159	SB159	SA159	

8. Command/AC Timing

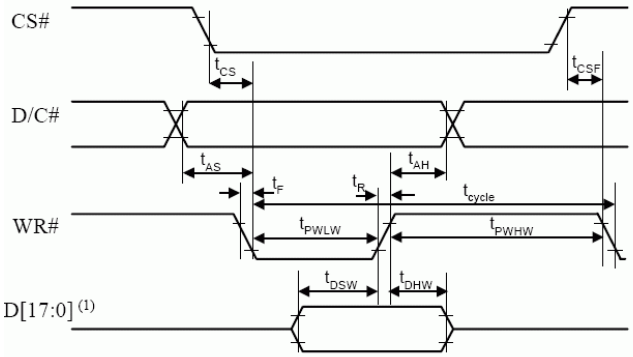
8.1 8080-Series MPU Parallel Interface Timing Characteristics

(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{DDIO}=1.6V, V_{CI} = 3.3V, T_A = 25°C)

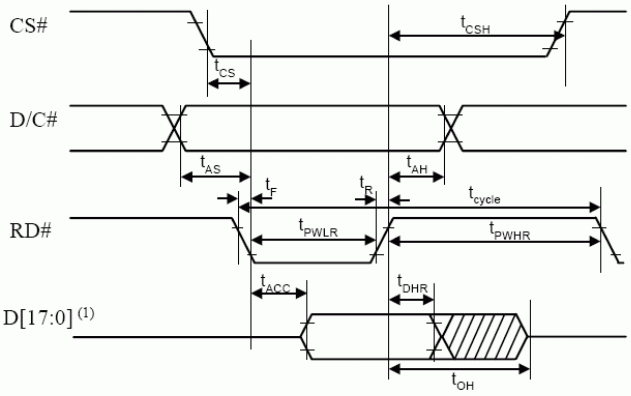
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	150	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

8080-series MCU parallel interface characteristics (Form 1)

Write cycle (Form 1)

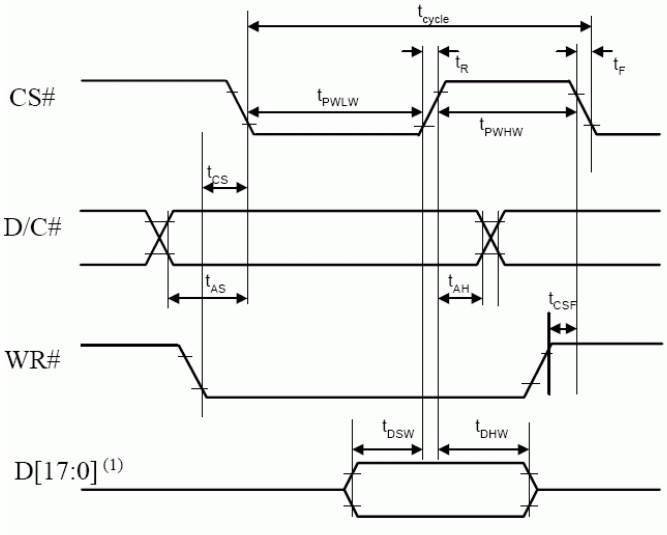


Read cycle (Form 1)

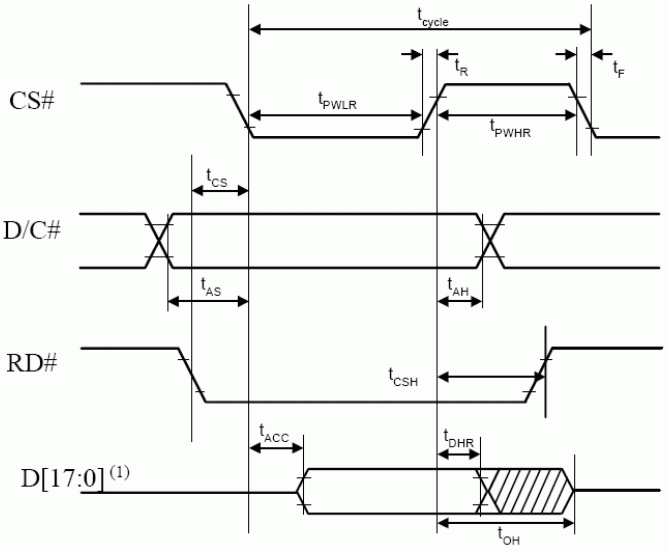


8080-series MCU parallel interface characteristics (Form 2)

Write cycle (Form 2)



Read cycle (Form 2)

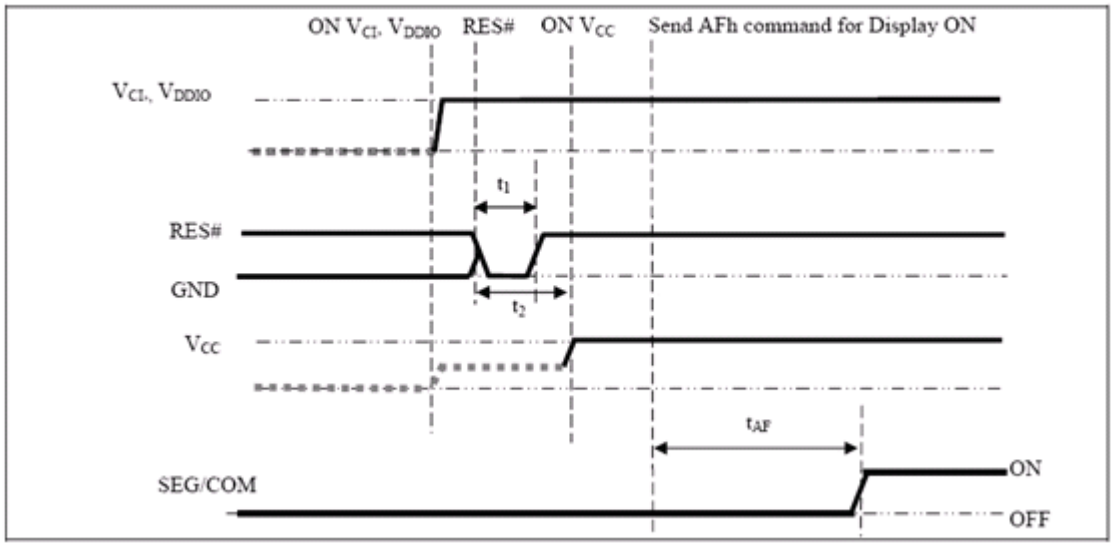


8.2 power on/ off sequence

8.2.1 Power on Sequence:

1. Power up VCI & VDDIO
2. After V_{CI}, V_{DDIO} become stable, set RES# pin LOW (logic low) for at least 100us (t_1) and then HIGH(logic high).
3. After set RES# pin LOW (logic low), wait for at least 100us (t_2). Then Power ON V_{CC}.
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 200ms(t_{AF}).

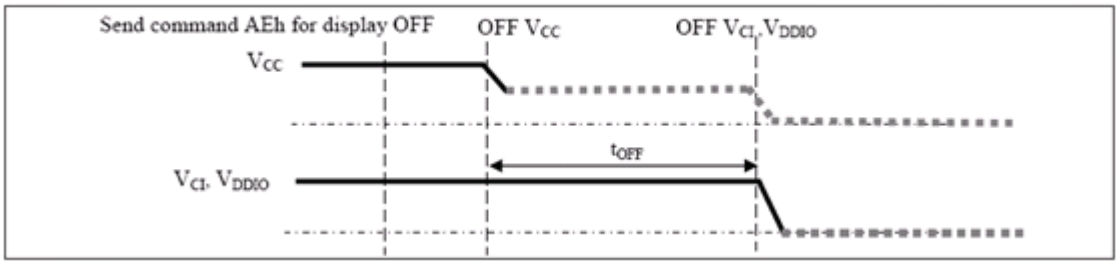
The Power ON sequence.



8.2.2 Power off Sequence:

1. Send command AEh for display OFF.
2. Power OFF V_{CC}.
3. Wait for t_{OFF}. Power OFF V_{CI},, V_{DDIO}.
   (Where Minimum t_{OFF}=80ms, Typical t_{OFF}=100ms)

The Power OFF sequence

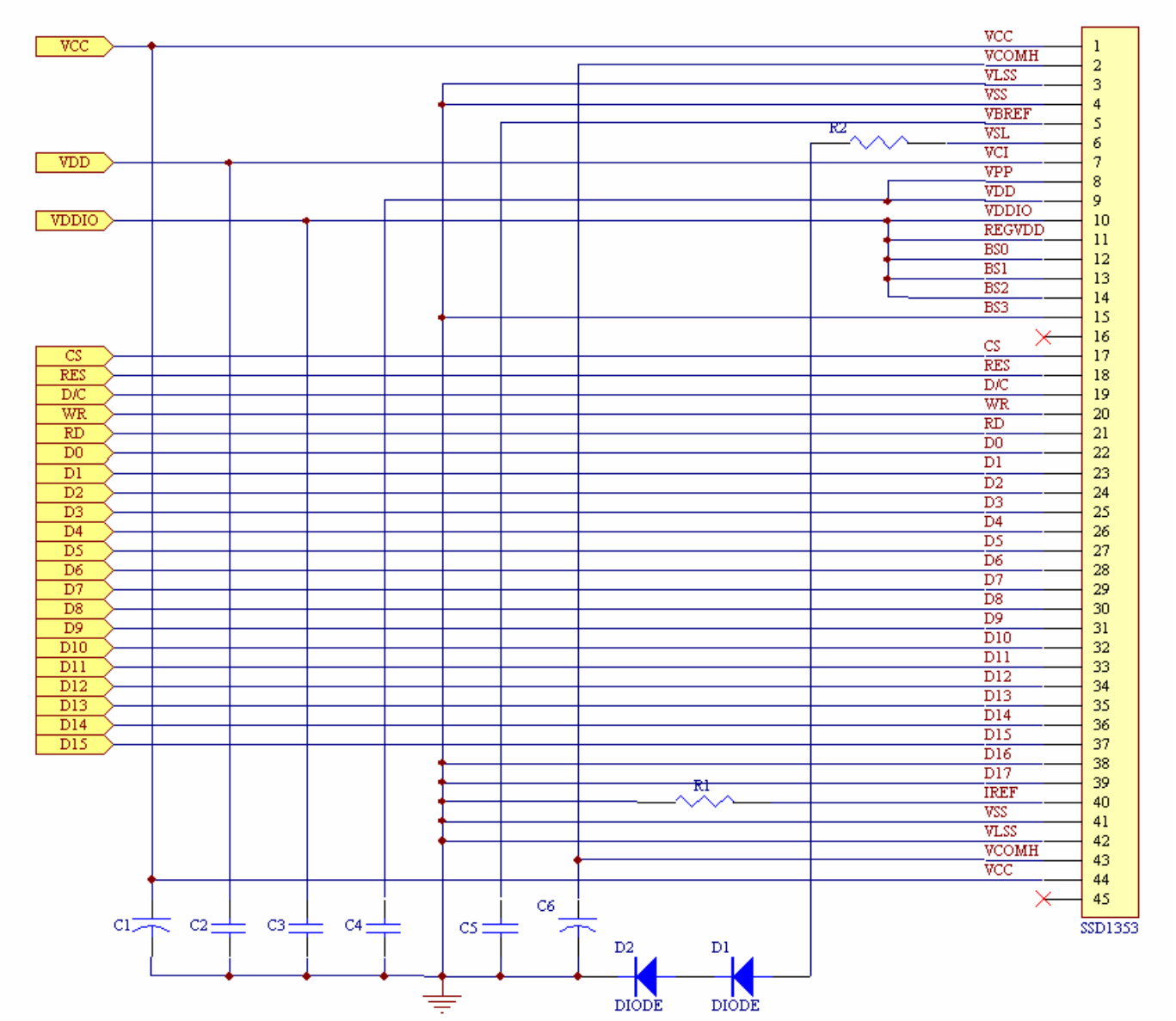


Note:

(1) Since an ESD protection circuit is connected between V_{CI}, V_{DDIO} and V_{CC}, V_{CC} becomes lower than V_{CI} whenever V_{CI},V_{DDIO} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in above figures.

(2) V_{CC} should be disabled when it is OFF.

8.3 APPLICATION CIRCUIT



Component:

C1, C6 : 4.7 uF/35V (Tantalum type) or VISHAY (572D475X0025A2T)
C2, C3, C4 : 1uF/16V(0603)
C5 : 0.1uF/16V(0603)
R1: 1.2M ohm (0603) 1%
R2: 50ohm 1/4W
D1 and D2: RB480K (ROHM)

This circuit is for 8080 16bits interface.

9. Optical Specification

Ta=25℃

Item		Symbol	Condition	Min	Typ.	Max.	Unit	Remark
Contrast Ratio		CR	θ=0° dark room	2000:1	--	--		Note1 Note2
View Angles			CR≧2	160	--	--	Degree	Note 3
Response Time				--	10	--	us	
Chromaticity	White	x	Brightness is on	Typ-0.04	0.31	Typ+0.04		Note4, Note1
		y			0.33			
	Red	x			0.66			
		y			0.33			
	Green	x			0.30			
		y			0.63			
	Blue	x			0.14			
		y			0.18			
Luminance		L		60	80	--	cd/m^2	Note1 Note5
Normal mode power consumption				--	663	697	mW	All pixels on
Standby mode power consumption				--	51	85	mW	Standby mode 10% pixels on
Normal mode current				--	39	41	mA	All pixels on
Standby mode current				--	3	5	mA	Standby mode 10% pixels on

Normal mode condition :

- Driving Voltage : 17V
- Contrast setting : 0x0f
- Frame rate : 85Hz
- Duty setting : 1/128

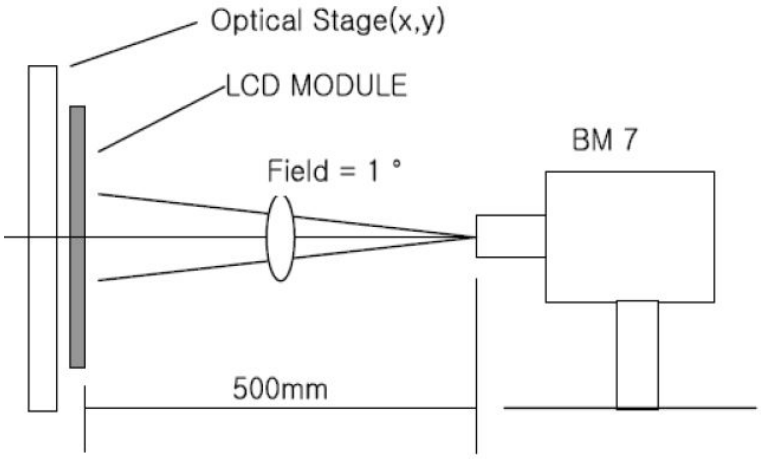
Standby mode condition :

- Driving Voltage : 17V
- Contrast setting : 0x05
- Frame rate : 85Hz
- Duty setting : 1/128

Note 1: Definition of optical measurement system.

Temperature = 25℃(±3℃)

LED back-light: ON, Environment brightness < 150 lx

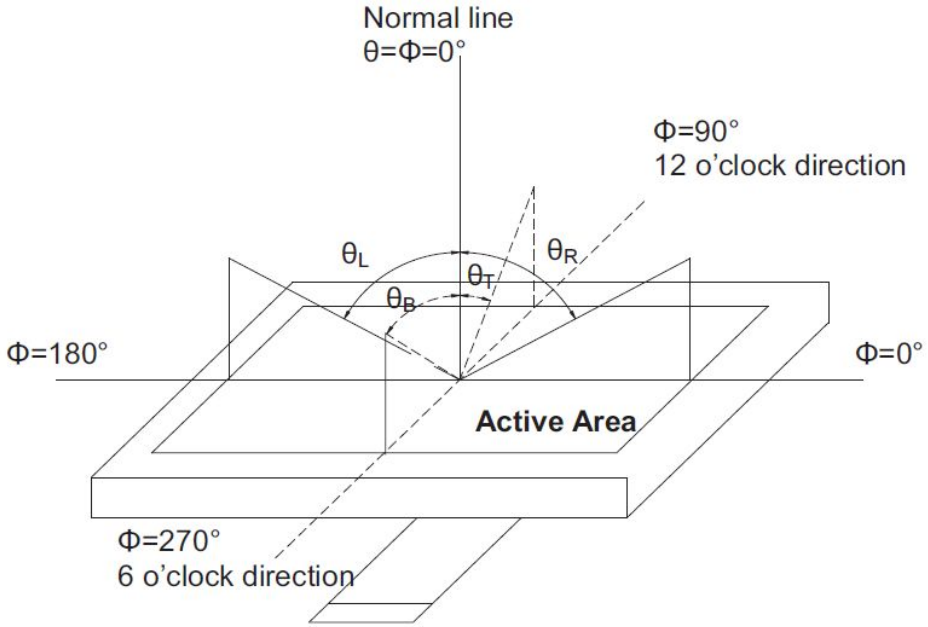


Note 2: Contrast ratio is defined as follow:

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

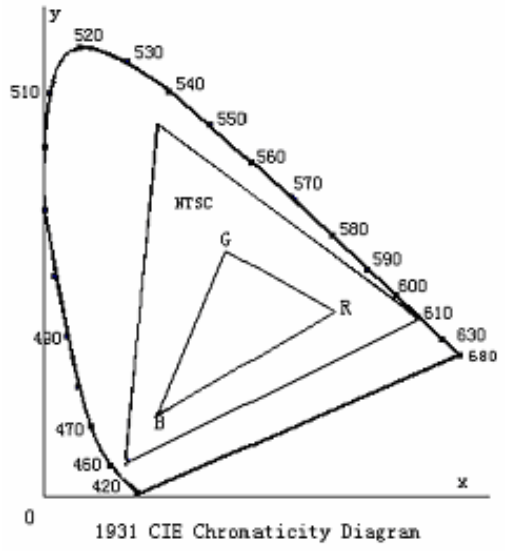
Note 3: Viewing angle range is defined as follow:

Viewing angle is measured at the center point of the OLED.



Note 4: Color chromaticity is defined as follow: (CIE1931)

Color coordinates measured at center point of OLED.



$$S = \frac{\text{area of RGB triangle}}{\text{area of NTSC triangle}} \times 100\%$$

Note 5: Luminance is defined as follow:

Luminance is defined as the brightness of all pixels “White” at the center of display area on optimum contrast.

10. Environmental / Reliability Tests

No	Test Item	Condition	Judgment criteria
1	High Temp Operation	Ts=+70℃, 120hrs	Per table in below
2	Low Temp Operation	Ta=-40℃, 120hrs	Per table in below
3	High Temp Storage	Ta=+85℃, 240hrs	Per table in below
4	High Temp & High Humidity Storage	Ta=+65℃, 90% RH 96 hours	Per table in below (polarizer discoloration is excluded)
5	Thermal Shock (Non-operation)	-40° C ~85° C (-40° C /30min; transit/3min;85° C /30min; transit /3min) 1cycle: 66min, 20 cycles	Per table in below
6	ESD (Operation)	Air discharge model, ±8kV, 10 times	Per table in below
7	Vibration (Non-operation)	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	Per table in below
8	Package Drop Test	Height: 120cm Sequence : 1 angle, 3 edges and 6 faces Cycles: 1	Per table in below

INSPECTION	CRITERION(after test)
Appearance	No Crack on the FPC, on the OLED Panel
Alignment of OLED Panel	No Bubbles in the OLED Panel No other Defects of Alignment in Active area
Electrical current	Within device specifications
Function / Display	No Broken Circuit, No Short Circuit or No Black line No Other Defects of Display

11. Precautions for Use of OLED Modules

11.1 Safety

The liquid crystal in the OLED is poisonous. Do not put it in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and water.

11.2 Handling

A. The OLED and touch panel is made of plate glass. Do not subject the panel to mechanical shock or to excessive force on its surface.
B. Do not handle the product by holding the flexible pattern portion in order to assure the reliability
C. Transparency is an important factor for the touch panel. Please wear clear finger sacks, gloves and mask to protect the touch panel from finger print or stain and also hold the portion outside the view area when handling the touch panel.
D. Provide a space so that the panel does not come into contact with other components.
E. To protect the product from external force, put a covering lens (acrylic board or similar board) and keep an appropriate gap between them.
F. Transparent electrodes may be disconnected if the panel is used under environmental conditions where dew condensation occurs.
G. Property of semiconductor devices may be affected when they are exposed to light, possibly resulting in IC malfunctions.
H. To prevent such IC malfunctions, your design and mounting layout shall be done in the way that the IC is not exposed to light in actual use.

11.3 Static Electricity

A. Ground soldering iron tips, tools and testers when they are in operation.
B. Ground your body when handling the products.
C. Power on the OLED module before applying the voltage to the input terminals.
D. Do not apply voltage which exceeds the absolute maximum rating.
E. Store the products in an anti-electrostatic bag or container.

11.4Storage

A. Store the products in a dark place at +25℃±10℃ with low humidity (40% RH to 60% RH). Don't expose to sunlight or fluorescent light.
B. Storage in a clean environment, free from dust, active gas, and solvent.

11.5 Cleaning

A. Do not wipe the touch panel with dry cloth, as it may cause scratch.
B. Wipe off the stain on the product by using soft cloth moistened with ethanol. Do not allow ethanol to get in between the upper film and the bottom glass. It may cause peeling issue or defective operation. Do not use any organic solvent or detergent other than ethanol.

11.6 Cautions for installing and assembling

Bezel edge must be positioned in the area between the Active area and View area. The bezel may press the touch screen and cause activation if the edge touches the active area. A gap of approximately 0.5mm is needed between the bezel and the top electrode. It may cause unexpected activation if the gap is too narrow. There is a tolerance of 0.2 to 0.3mm for the outside dimensions of the touch panel and tail. A gap must be made to absorb the tolerance in the case and connector.