DLC Display Co., Limited

德爾西顯示器有限公司

MODEL No: DLC0145BNOF

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Record of Revision

Date	Revision No.	Summary
2010-07-13	1.0	Rev 1.0 was issued
2011-03-28	2.0	Update Outline drawing, Interface signals and Schematic of OLED module system

1. Scope

This data sheet is to introduce the specification of DLC0145BNOF, passive matrix OLED module. It is composed of an OLED panel, driver ICs. The 1.45″ display area contains 160(RGB) x 128 pixels.

2. Application

Digital equipments which need color display, mobile phone, mobile navigator/video systems.

3. General Information

Item	Contents	Unit
Size	1.45	inch
Resolution	160(RGB) x 128	/
Technology type	Passive OLED	/
Display Color	262,144 Colors (Maximum)	
Interface	6-/8-/9-bit RGB 6800XX/80XX parallel, 4-wire SPI	
Pixel size	0.04x0.164	
Pixel pitch	0.06x0.18	mm
Outline Dimension (W x H x D)	35.80 × 30.80 × 1.60	mm
Active Area	28.78 × 23.024	mm
Drive Duty	1/128 Duty	/
Driver IC	SEPS525-F00	
Operating Temperature	-30℃~+70℃	
Storage Temperature	-40℃~＋80℃	

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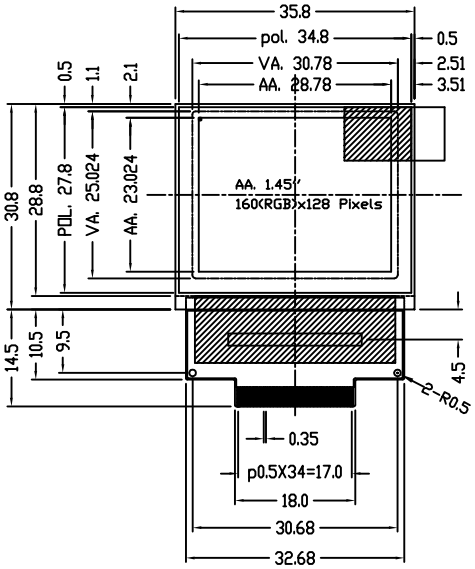
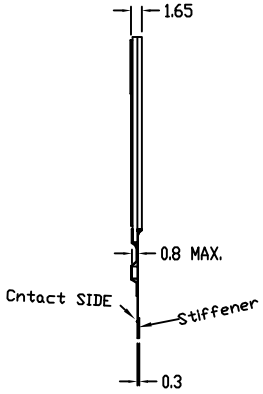
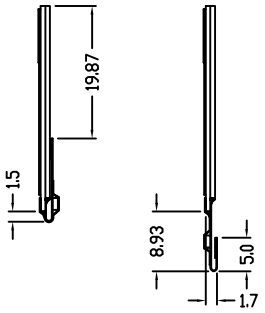
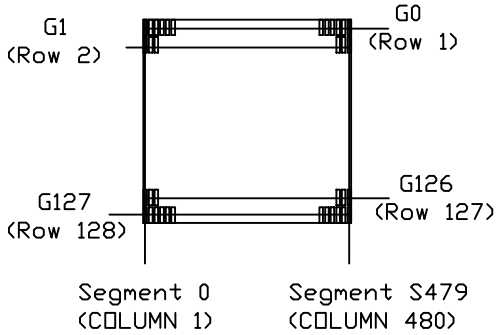
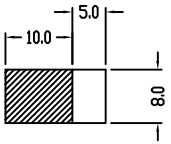
No:	PIN NAME
1	N.C.
2	VSDH
3	VDDH
4	VSSH
5	IREF
6	□SCA2
7	□SCA1
8	VDDI□
9	VSYNC□
10	VSYNC
11	HSYNC
12	D□TCLK
13	ENABLE
14	CPU
15	PS
16	D17
17	D16
18	D15
19	D14
20	D13
21	D12
22	D11
23	D10
24	D9
25	RS
26	CSB
27	RDB
28	WRB
29	RESETB
30	VSS
31	VDD
32	VSSH
33	VDDH
34	VSDH
35	N.C.

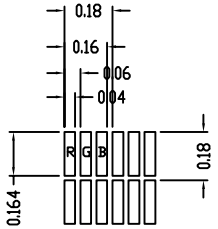












SCALE 40 : 1

NOTES:

1.DRIVE IC: SEPS525

2.Die Size : 19660um X 1850um

3.COF Number : SEPS525F

4.Interface :6-/8-/9-/bitsRGB I/F, 68XX/80XX Parallel,4-wire SPI

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DRAWN BY:	TITLE: DLC0145BNOF		
CHECKED BY:			
APPROVED BY:	DWG NO:	SCALE:	
		UNIT: mm	
CONFIRMED BY:	DWG NAME:	SHEET NO: 0F	

5. Interface signals

<table>
<tr><th>No</th><th>Symbol</th><th>Description</th><th>Remarks</th></tr>
<tr><td>1</td><td>NC</td><td>No Connection</td><td></td></tr>
<tr><td>2</td><td>VSDH</td><td>Data Driver Ground</td><td></td></tr>
<tr><td>3</td><td>VDDH</td><td>Data, Scan Driver Power Supply.</td><td></td></tr>
<tr><td>4</td><td>VSSH</td><td>Scan Driver Ground</td><td></td></tr>
<tr><td>5</td><td>IREF</td><td>Current Reference for Brightness Adjustment
Tie 68KΩ resistor to VSS.</td><td></td></tr>
<tr><td>6</td><td>OSCA2</td><td rowspan="2">Fine adjustment for oscillation
Tie 10 KΩ resistor to OSCA1 between OSCA2.
When the external clock mode is selected, OSCA1 is used external clock input.</td><td></td></tr>
<tr><td>7</td><td>OSCA1</td><td></td></tr>
<tr><td>8</td><td>VDDIO</td><td>MPU I/F PAD Power Supply</td><td></td></tr>
<tr><td>9</td><td>VSYNCO</td><td rowspan="5">RGB Mode Functional Pins
VSYNCO: Vertical Sync. Output
VSYNC: Vertical Sync. Input
HSYNC: Horizontal Sync. Input
DOTCLK: Dot Clock Input
ENABLE: Video Enable Input</td><td></td></tr>
<tr><td>10</td><td>VSYNC</td><td></td></tr>
<tr><td>11</td><td>HSYNC</td><td></td></tr>
<tr><td>12</td><td>DOTCLK</td><td></td></tr>
<tr><td>13</td><td>ENABLE</td><td></td></tr>
<tr><td>14</td><td>CPU</td><td>Selects the CPU type
Low: 80-series CPU, High: 68-Series CPU.</td><td></td></tr>
<tr><td>15</td><td>PS</td><td>Selects parallel/Serial interface type
Low: serial, High: parallel</td><td></td></tr>
<tr><td>16-24</td><td>D17-D9</td><td>Host Data Input/Output Bus
These pins are 9-bit bi-directional data bus to be connected with MCU data bus.
<table>
<tr><td>PS</td><td>Description</td></tr>
<tr><td>1</td><td>8_bit bus : D[17:10]
9_bit bus : D[17:9]</td></tr>
<tr><td>0</td><td>D[17] SCL : Synchronous clock input
D[16] SDI : Serial data input
D[15] SDO : Serial data output</td></tr>
<tr><td colspan="2">Fix unused pins to the VSS level.</td></tr>
</table></td><td></td></tr>
<tr><td>25</td><td>RS</td><td>Selects the data/command
Low: command, High: parameter/data</td><td></td></tr>
<tr><td>26</td><td>CSB</td><td>Chip Select
Low: SEPS525 is selected and can be accessed.
High: SEPS525 is not selected and cannot be accessed.</td><td></td></tr>
<tr><td>27</td><td>RDB</td><td>Read or Read/Write Enable
80-system bus interface: read strobe signal (active low).
68-system bus interface: bus enable strobe (active high).
When serial mode, fix it to VDD or VSS level.</td><td></td></tr>
<tr><td>28</td><td>WRB</td><td>Write or Read/Write Select
80-system bus interface: write strobe signal (active low).
68-system bus interface: read/write select.
Low: write, High: read.
When serial mode, fix it to VDD or VSS level</td><td></td></tr>
<tr><td>29</td><td>RESETB</td><td>Chip Reset
Reset SEPS525 (active low)</td><td></td></tr>
<tr><td>30</td><td>VSS</td><td>Logic Ground</td><td></td></tr>
<tr><td>31</td><td>VDD</td><td>Logic Power Supply.</td><td></td></tr>
</table>

32	VSSH	Scan Driver Ground	
33	VDDH	Data, Scan Driver Power Supply.	
34	VSDH	Data Driver Ground	
35	NC	No Connection	

6. Absolute maximum Ratings

6.1. Electrical Absolute max. ratings

Parameter	Symbol	MIN	MAX	Unit	Remark
Supply Voltage	VDD	-0.3	4.0	V	
supply Voltage for I/O pins	VDDIO	-0.3	4.0	V	
Driver supply voltage	VDDH	-0.3	16.0	V	

6.2. Environment Conditions

Item	Symbol	MIN	MAX	Unit	Remark
Operating Temperature	TOPR	-30	70	℃	
Storage Temperature	TSTG	-40	80	℃	

7. Electrical Specifications

7.1 Electrical characteristics

GND=0V, Ta=25℃

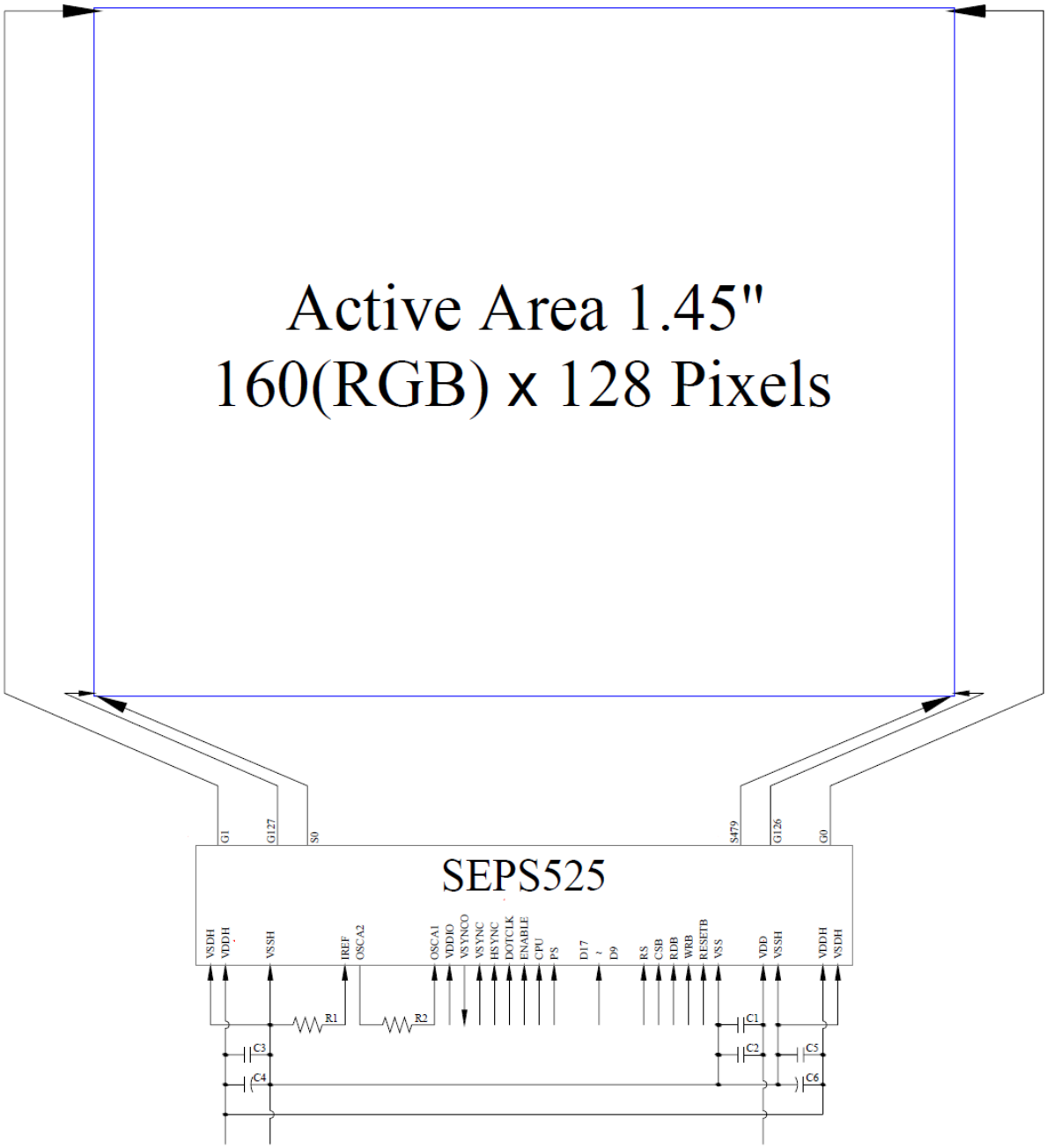
Item	Symbol	MIN	TYP	MAX	Unit	Remark
Supply Voltage	VDD	2.6	2.8	3.3	V	
supply Voltage for I/O pins	VDDIO	1.6	2.8	3.3	V	
Driver supply voltage	VDDH	-	13.0	-	V	Note1
Input Signal Voltage	VIL	0	--	0.4	V	
	VIH	0.8VDD	--	VDD	V	
output Signal Voltage	VOL	-	-	0.4	V	
	VOH	VDD-0.4	-	=	V	
Operating Current for VDD	IVDD	--	2.5	3.5	mA	Note 2
		--	2.5	3.5	mA	Note 3
Operating Current for Vcc	Icc	--	16	19	mA	Note 2
		--	27	32	mA	Note 3

Note 1: Brightness (Lbr) and Driver Supply Voltage (VCC) are subject to the change of the panel characteristics and the customer's request.

Note 2: VDD = 2.8V, VCC = 13V, Software Initial Setting follow Chapter 8.6 "Initial Code", 50% Display Area Turn on.

Note 3: VDD = 2.8V, VCC = 13V, Software Initial Setting follow Chapter 8.6 "Initial Code", 100% Display Area Turn on.

7.2 Schematic of OLED module system



MCU Interface Selection: PS, CPU
Pins connected to MCU interface: D17~D9, RS, CSB, RDB, WRB, RESETB, ENABLE, DOTCLK, HSYNC, and VSYNC
* When RGB mode is used, D[17:12], ENABLE, DOTCLK, HSYNC, and VSYNC should follow the 6-bit RGB interface instruction. Otherwise, ENABLE, DOTCLK, HSYNC, and VSYNC these four input signal should be tie to VDDIO level.

C1, C3, C5: 0.1μF
C2: 4.7μF
C4, C6: 4.7μF / 25V Tantalum Capacitor
R1: 68kΩ
R2: 10kΩ

8. Command/AC Timing

8.1 68XX-Series MPU Parallel Interface Timing Characteristics

8.1.1 WRITING TIMING

(VDD = 2.8V, Ta = 25℃)

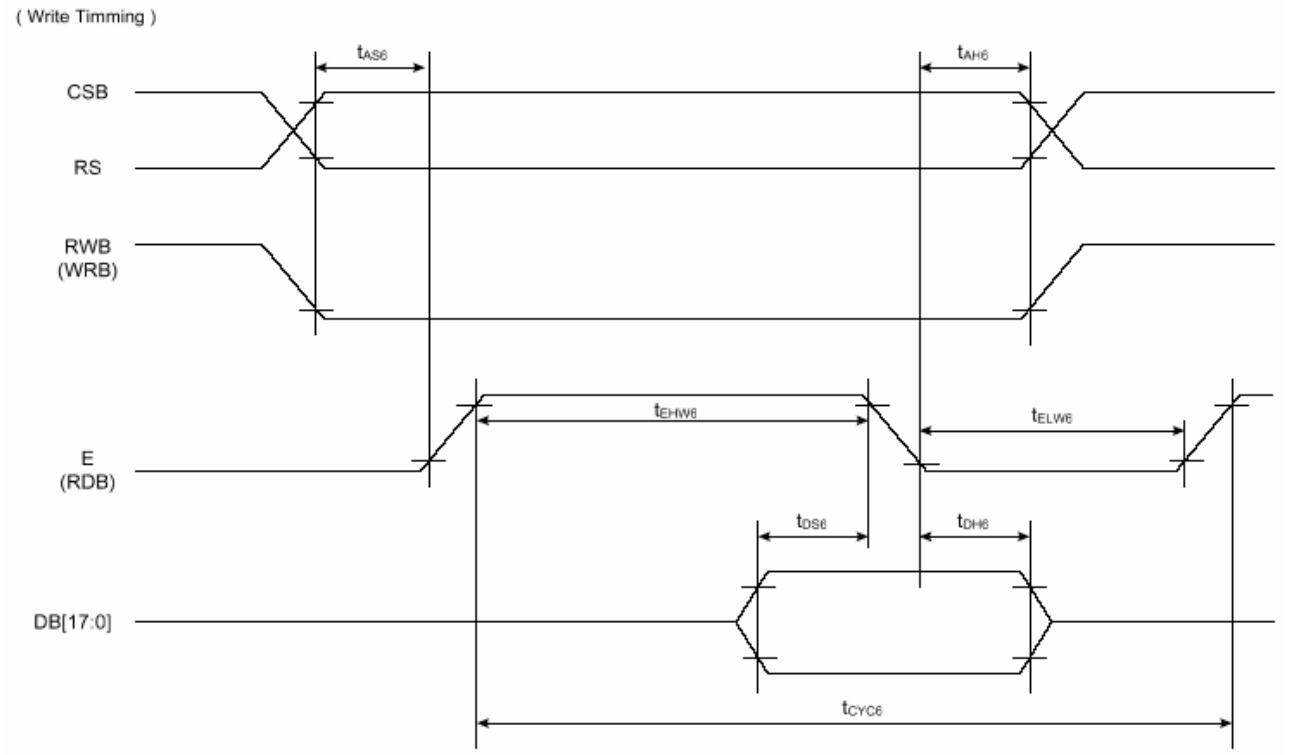
Item	Symbol	MIN	TYP	MAX	Unit	Remark
Address hold timing Address setup timing	tAH6 tAS6	5 5	-	-	ns	CSB RS
System cycle timing Write “L” pulse width Write “H” pulse width	tCYC6 tELW6 tEHW6	100 45 45	-	-	ns	E
Data setup timing Data hold Timing	tDS6 tDH6	40 10	-	-	ns	DB[17:0]

8.1.2 READ TIMING

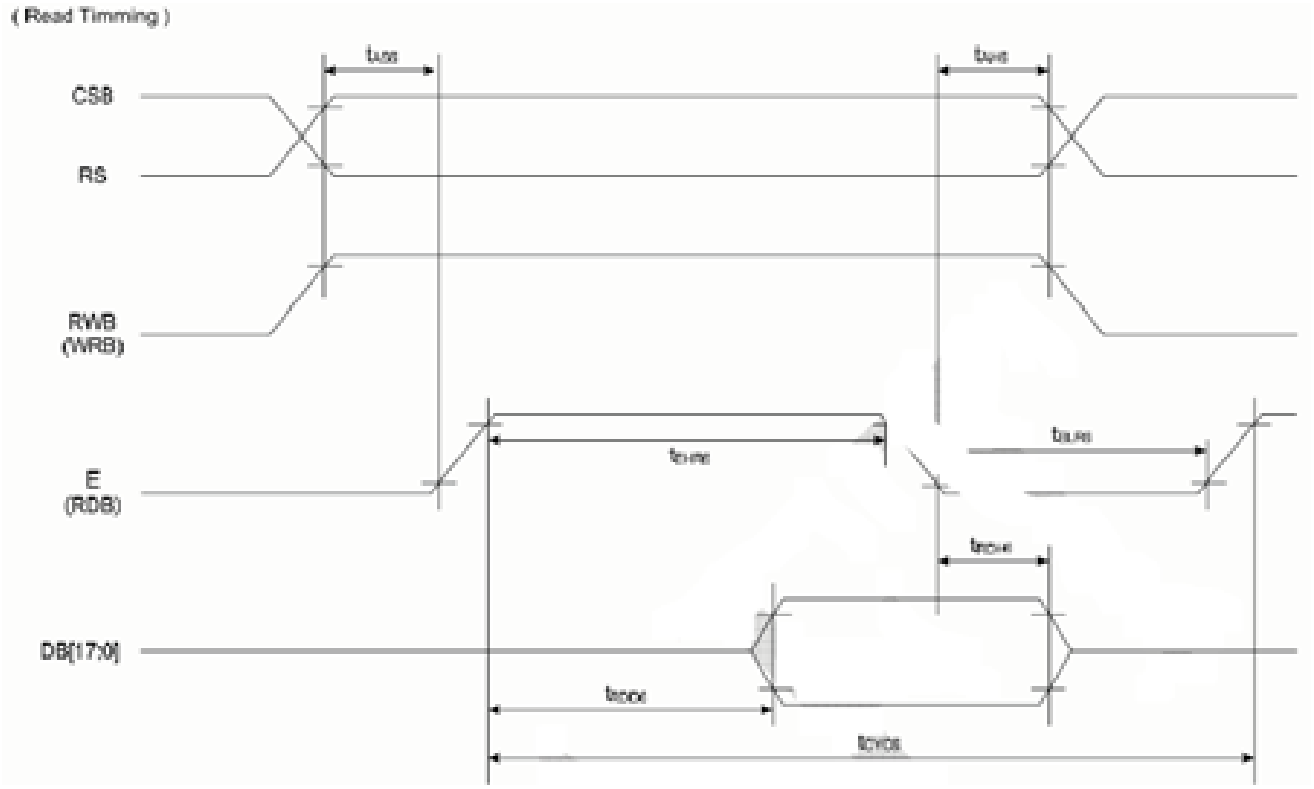
Item	Symbol	MIN	TYP	MAX	Unit	Remark
Address hold timing Address setup timing	tAH6 tAS6	10 10		-	ns	CSB RS
System cycle timing Read “L” pulse width read “H” pulse width	tCYC6 tELW6 tEHW6	200 90 90			ns	E
Data setup timing Data hold Timing	trdd6 tedh6	0		70	ns	C_L = 15pF DB[17:0]

All the timing reference is 10% and 90% of VDD.

(Write Timming)



(Read Timming)



8.2 80XX-Series MPU Parallel Interface Timing Characteristics

8.2.1 WRITING TIMING (VDD = 2.8V, Ta = 25℃)

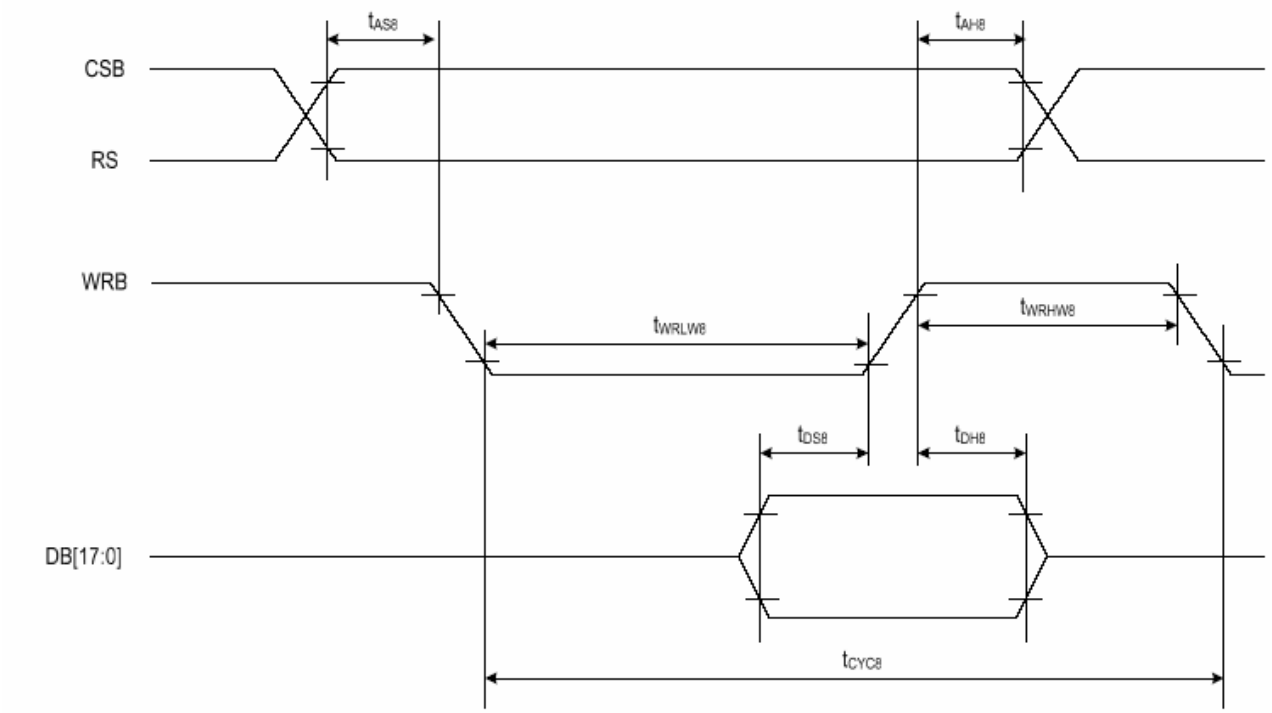
Item	Symbol	MIN	TYP	MAX	Unit	Remark
Address hold timing Address setup timing	tAH8 tAS8	5 5		-	ns	CSB RS
System cycle timing Write “L” pulse width Write “H” pulse width	tCYC8 tELW8 tEHW8	100 45 45			ns	WRB
Data setup timing Data hold Timing	tDS8 tDH8	30 10		-	ns	DB[17:0]

8.2.2 READ TIMING

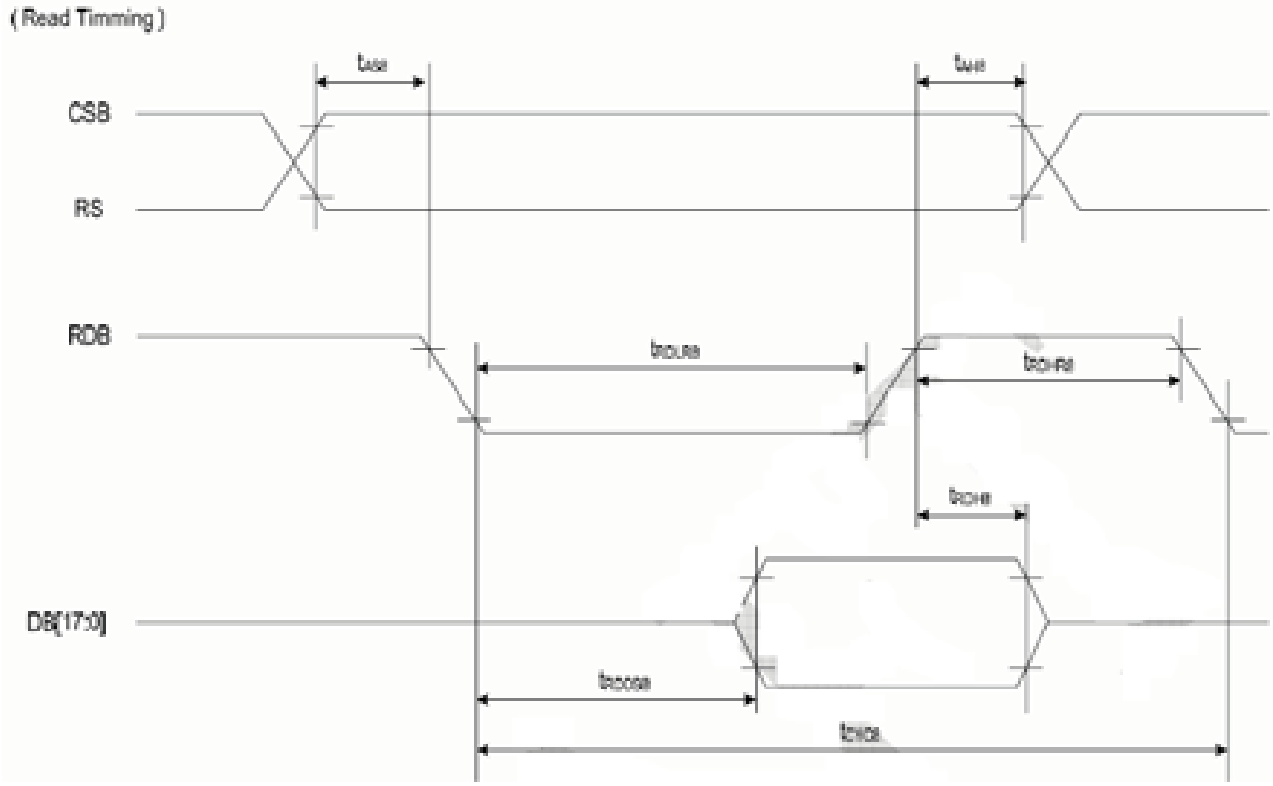
Item	Symbol	MIN	TYP	MAX	Unit	Remark
Address hold timing Address setup timing	tAH8 tAS8	10 10		-	ns	CSB RS
System cycle timing Read “L” pulse width read “H” pulse width	tCYC8 tELW8 tEHW8	200 90 90			ns	RDB
Data setup timing Data hold Timing	Trdd8 Tedh8	0		60	ns	C_L = 15pF DB[17:0]

All the timing reference is 10% and 90% of VDD.

(Write Timming)



(Read Timming)

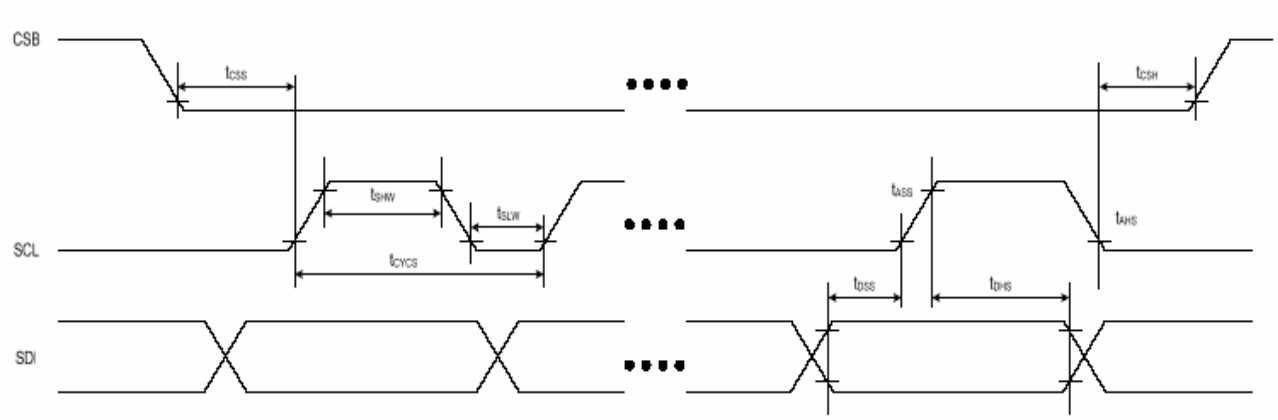


8.3 AC Characteristics INTERFACE

(VDD = 2.8V, Ta = 25℃)

Item	Symbol	MIN	MAX	Unit	Remark
Serial clock cycle	t_{CYCS}	60	-	ns	SCL
SCL "H" pulse width	t_{SHW}	25			
SCL "L" pulse width	t_{SLW}	25			
CSB-SCL timing	t_{CSS}	25	-	ns	CSB
CSB-hold timing	t_{CSH}	25			
Data setup timing	t_{DSS}	25	--	ns	SDI
Data hold Timing	t_{DHS}	25			

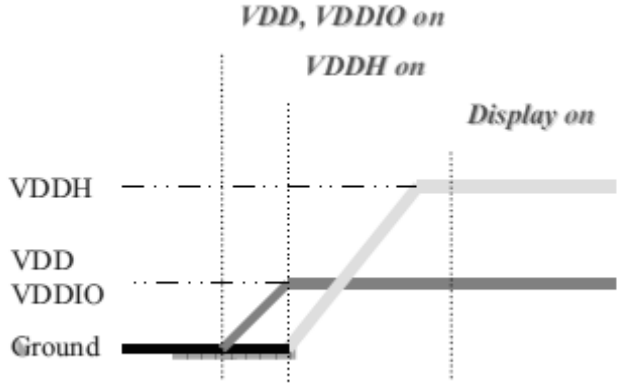
NOTE: All the timing reference is 10% and 90% of VDD



8.4 Power down and Power up Sequence

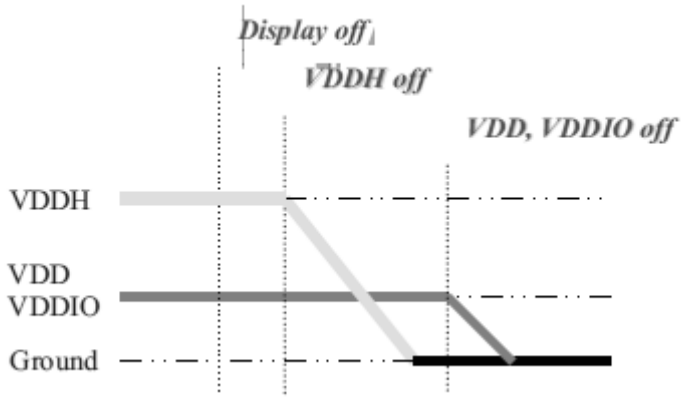
8.4.1 Power up Sequence:

1. Power up VDD,VDDIO
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up VDDH
6. Delay 100ms (When VDDH is stable)
7. Send Display on command



8.4.2 Power down Sequence:

1. Send Display off command
2. Power down VDDH
3. Delay 100ms (When VDDH is reach 0 and panel is completely discharges)
4. Power down VDD



8.5 Reset Circuit

When RESETB input is low, the chip is initialized with the following status:

1. Frame frequency: 90Hz
2. OSC: internal OSC
3. Internal OSC: ON
4. DDRAM write horizontal address: MX1 = 00h, MX2 = 9Fh
5. DDRAM write vertical address: MY1 = 00h, MY2 = 7Fh
6. Display data RAM write: HC = 1, VC = 1, HV = 0
7. RGB data swap: OFF
8. Row scan shift direction: G0, G1, … , G126, G127
9. Column data shift direction: S0, S1, … , S478, S479
10. Display ON/OFF: OFF
11. Panel display size: FX1 = 00h, FX2 = 9Fh, FY1 = 00h, FY2 = 7Fh
12. Display data RAM read column/row address: FAC = 00h, FAR = 00h
13. Precharge time(R/G/B): 0 clock
14. Precharge current(R/G/B): 0 uA
15. Driving current(R/G/B): 0 uA

8.6 Initial Code

```
//OSC control
//EXPORT1 internal clock and OSC operates with external resister
Write_Register(0x02);
Write_Parameter(0x01);
//REDUCE_CURRENT
//Reduced driving current : normal
//Power save mode:normal
Write_Register(0x04);
Write_Parameter(0x00);
//CLOCK_DIV
//OSC frequency setting : 90Hz
//Display frequency divide ration:1
Write_Register(0x03);
Write_Parameter(0x30);
//IREF_Reference volt. controlled by External resister
//_RGB current and precharge time,current separate control
Write_Register(0x80);
Write_Parameter(0x00);
//PRECHARGE_TIME_R
//1 Precharge Time
Write_Register(0x08);
Write_Parameter(0x01);
//PRECHARGE_TIME_G
//1 Precharge Time
Write_Register(0x09);
Write_Parameter(0x01);
//PRECHARGE_TIME_B
//1 Precharge Time
Write_Register(0x0A);
Write_Parameter(0x02);
//PRECHARGE_CURRENT_R
Write_Register(0x0B);
Write_Parameter(0x0C);
//PRECHARGE_CURRENT_G
Write_Register(0x0C);
Write_Parameter(0x19);
//PRECHARGE_CURRENT_B
Write_Register(0x0D);
Write_Parameter(0x15);
//DRIVING_CURRENT_R
Write_Register(0x10);
Write_Parameter(0x32);
//DRIVING_CURRENT_G
Write_Register(0x11);
Write_Parameter(0x27);
//DRIVING_CURRENT_B
/Write_Register(0x12);
Write_Parameter(0x3B);
//Display mode set
//RGB,column=0_159,column data display control=Normal Dispaly
Write_Register(0x13);
Write_Parameter(0x00);
//External interface mode =MPU
Write_Register(0x14);
Write_Parameter(0x01);
//MEMORY_WRITE_MODE
//6btis Triple transfer,262K support ,Horizontal address counter is increased,Vertical
address
//counter is increased,The data is continuously written horizontally
Write_Register(0x16);
```

```
Write_Parameter(0x76);
//Memory addrss setting range 0x17~0x19 160x128
Write_Register(0x17); //column start
Write_Parameter(0x00);
Write_Register(0x18); //column end
Write_Parameter(0x9F);
Write_Register(0x19); //row start
Write_Parameter(0x00);
Write_Register(0x1A); //row end
Write_Parameter(0x7F);
//Memory Start Address set 0x20~0x21
Write_Register(0x20); // X
Write_Parameter(0x00);
Write_Register(0x21); // Y
Write_Parameter(0x00);
//DUTY
Write_Register(0x28);
Write_Parameter(0x7F); //128
//Display Start LIne
Write_Register(0x29);
Write_Parameter(0x00);
//DDRAM Read Address Start point 0x2E~0x2F
Write_Register(0x2E); // X
Write_Parameter(0x00);
Write_Register(0x2F); // Y
Write_Parameter(0x00);
//Display Screen Saver Size 0x33~0x36
Write_Register(0x33); //Display Screen Saver Columns Start
Write_Parameter(0x00);
Write_Register(0x34); //Display Screen Saver Columns End
Write_Parameter(0x9F);
Write_Register(0x35); //Display Screen Saver Row Start
Write_Parameter(0x00);
Write_Register(0x36); //Display Screen Saver Row End
Write_Parameter(0x7F);
Write_Register(0x06); //Display ON
Write_Parameter(0x01);
```

9. Optical Specification

Ta=25℃

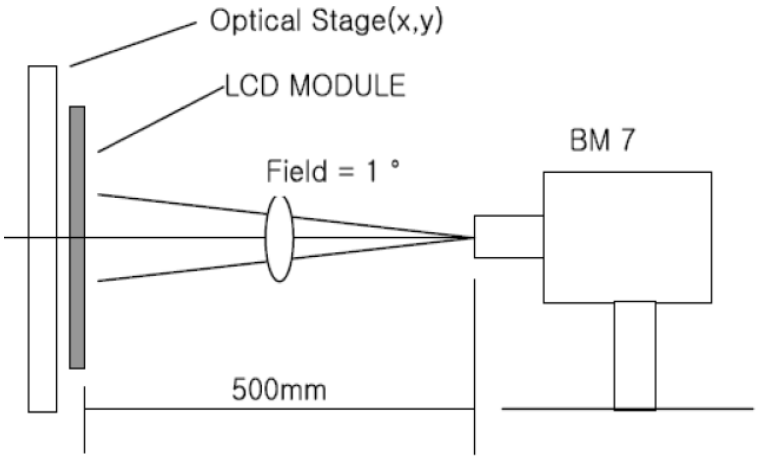
Item		Symbol	Condition	Min	Typ.	Max.	Unit	Remark
Contrast Ratio		CR	θ=0°		2000	-		Note1 Note2
View Angles		ΘT	CR≧2	80		-	Degree	Note 3
		ΘB		80		-		
		ΘL		80		-		
		θR		80		-		
Chromaticity	White	x	Brightness is on	Typ-0.04	0.30	Typ+0.04		Note4, Note1
		y			0.33			
	Red	x			0.64			
		y			0.34			
	Green	x			0.31			
		y			0.63			
	Blue	x			0.14			
		y			0.16			
Luminance		L		70	100	-	cd/m^2	Note1 Note5

Note : Optical measurement with polarizer is taken @ VDD, VDDIO = 2.8V, VDDH = 13V, and the software initial setting with section 8.6 Reference

Note 1: Definition of optical measurement system.

Temperature = 25℃(±3℃)

LED back-light: ON, Environment brightness < 150 lx

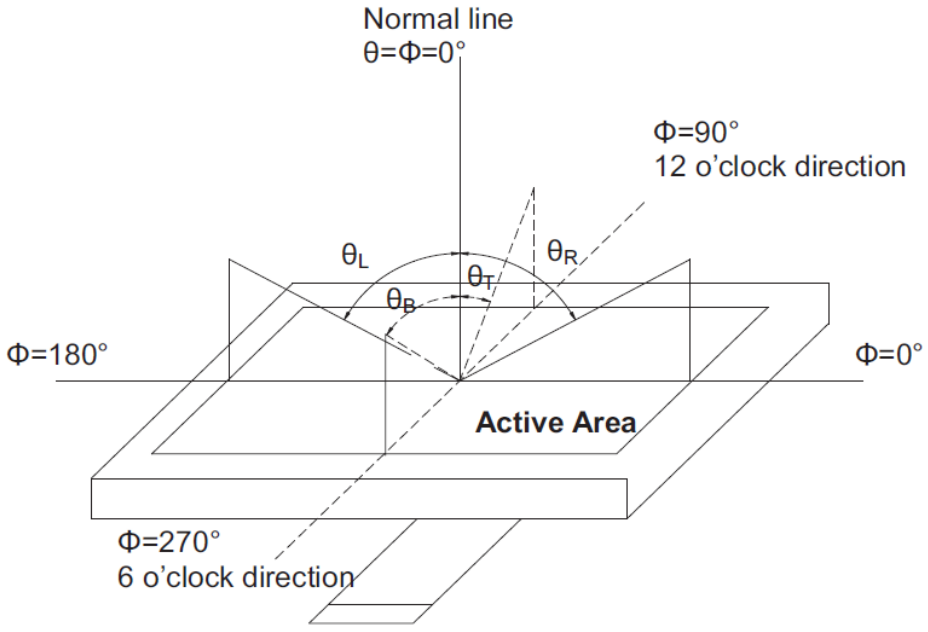


Note 2: Contrast ratio is defined as follow:

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

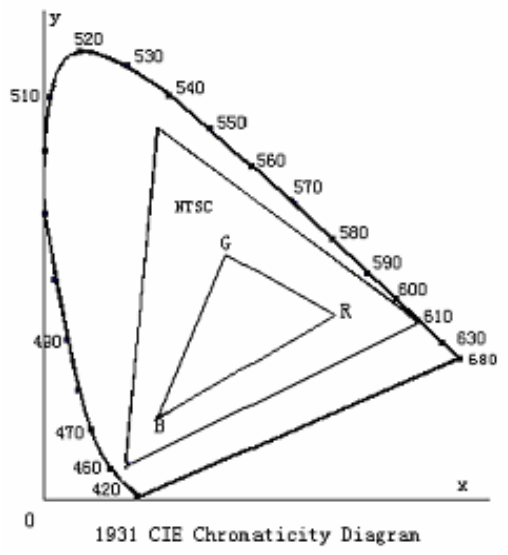
Note 3: Viewing angle range is defined as follow:

Viewing angle is measured at the center point of the OLED.



Note 4: Color chromaticity is defined as follow: (CIE1931)

Color coordinates measured at center point of OLED.



$$S = \frac{\text{area of RGB triangle}}{\text{area of NTSC triangle}} \times 100\%$$

Note 5: Luminance is defined as follow:

Luminance is defined as the brightness of all pixels “White” at the center of display area on optimum contrast.

10. Environmental / Reliability Tests

No	Test Item	Condition	Judgment criteria
1	High Temp Operation	Ts=+70℃, 120hrs	Per table in below
2	Low Temp Operation	Ta=-30℃, 120hrs	Per table in below
3	High Temp Storage	Ta=+80℃, 120hrs	Per table in below
4	Low Temp Storage	Ta=-40℃, 120hrs	Per table in below
5	High Temp & High Humidity Storage	Ta=+40℃, 90% RH 120 hours	Per table in below (polarizer discoloration is excluded)
6	Thermal Shock (Non-operation)	-40℃ 30 min~+85℃ 30 min, Change time:5min, 10 Cycles	Per table in below
7	ESD (Operation)	C=150pF, R=330Ω，5points/panel Air:±8KV, 5times; Contact:±4KV, 5 times;	Per table in below
8	Vibration (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z.	Per table in below
9	Shock (Non-operation)	60G 6ms, ±X,±Y,±Z 3times, for each direction	Per table in below
10	Package Drop Test	Height:80 cm, 1 corner, 3 edges, 6 surfaces	Per table in below

INSPECTION	CRITERION(after test)
Appearance	No Crack on the FPC, on the OLED Panel
Alignment of OLED Panel	No Bubbles in the OLED Panel No other Defects of Alignment in Active area
Electrical current	Within device specifications
Function / Display	No Broken Circuit, No Short Circuit or No Black line No Other Defects of Display

11. Precautions for Use of OLED Modules

11.1 Safety

The liquid crystal in the OLED is poisonous. Do not put it in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and water.

11.2 Handling

A. The OLED and touch panel is made of plate glass. Do not subject the panel to mechanical shock or to excessive force on its surface.
B. Do not handle the product by holding the flexible pattern portion in order to assure the reliability
C. Transparency is an important factor for the touch panel. Please wear clear finger sacks, gloves and mask to protect the touch panel from finger print or stain and also hold the portion outside the view area when handling the touch panel.
D. Provide a space so that the panel does not come into contact with other components.
E. To protect the product from external force, put a covering lens (acrylic board or similar board) and keep an appropriate gap between them.
F. Transparent electrodes may be disconnected if the panel is used under environmental conditions where dew condensation occurs.
G. Property of semiconductor devices may be affected when they are exposed to light, possibly resulting in IC malfunctions.
H. To prevent such IC malfunctions, your design and mounting layout shall be done in the way that the IC is not exposed to light in actual use.

11.3 Static Electricity

A. Ground soldering iron tips, tools and testers when they are in operation.
B. Ground your body when handling the products.
C. Power on the OLED module before applying the voltage to the input terminals.
D. Do not apply voltage which exceeds the absolute maximum rating.
E. Store the products in an anti-electrostatic bag or container.

11.4Storage

A. Store the products in a dark place at +25℃±10℃ with low humidity (40% RH to 60% RH). Don't expose to sunlight or fluorescent light.
B. Storage in a clean environment, free from dust, active gas, and solvent.

11.5 Cleaning

A. Do not wipe the touch panel with dry cloth, as it may cause scratch.
B. Wipe off the stain on the product by using soft cloth moistened with ethanol. Do not allow ethanol to get in between the upper film and the bottom glass. It may cause peeling issue or defective operation. Do not use any organic solvent or detergent other than ethanol.

11.6 Cautions for installing and assembling

Bezel edge must be positioned in the area between the Active area and View area. The bezel may press the touch screen and cause activation if the edge touches the active area. A gap of approximately 0.5mm is needed between the bezel and the top electrode. It may cause unexpected activation if the gap is too narrow. There is a tolerance of 0.2 to 0.3mm for the outside dimensions of the touch panel and tail. A gap must be made to absorb the tolerance in the case and connector.