DLC Display Co., Limited

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MODEL No: DLC0129AZOF-1

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Record of Revision

Date	Revision No.	Summary
2013-07-25	1.0	Rev 1.0 was issued

1. Scope

This data sheet is to introduce the specification of DLC0129AZOF-1, passive matrix OLED module. It is composed of an OLED panel, driver ICs and FPC. The1.29″ display area contains 128 x 96 pixels.

2. Application

Digital equipments which need display, instrumentation, remote control, electronic product.
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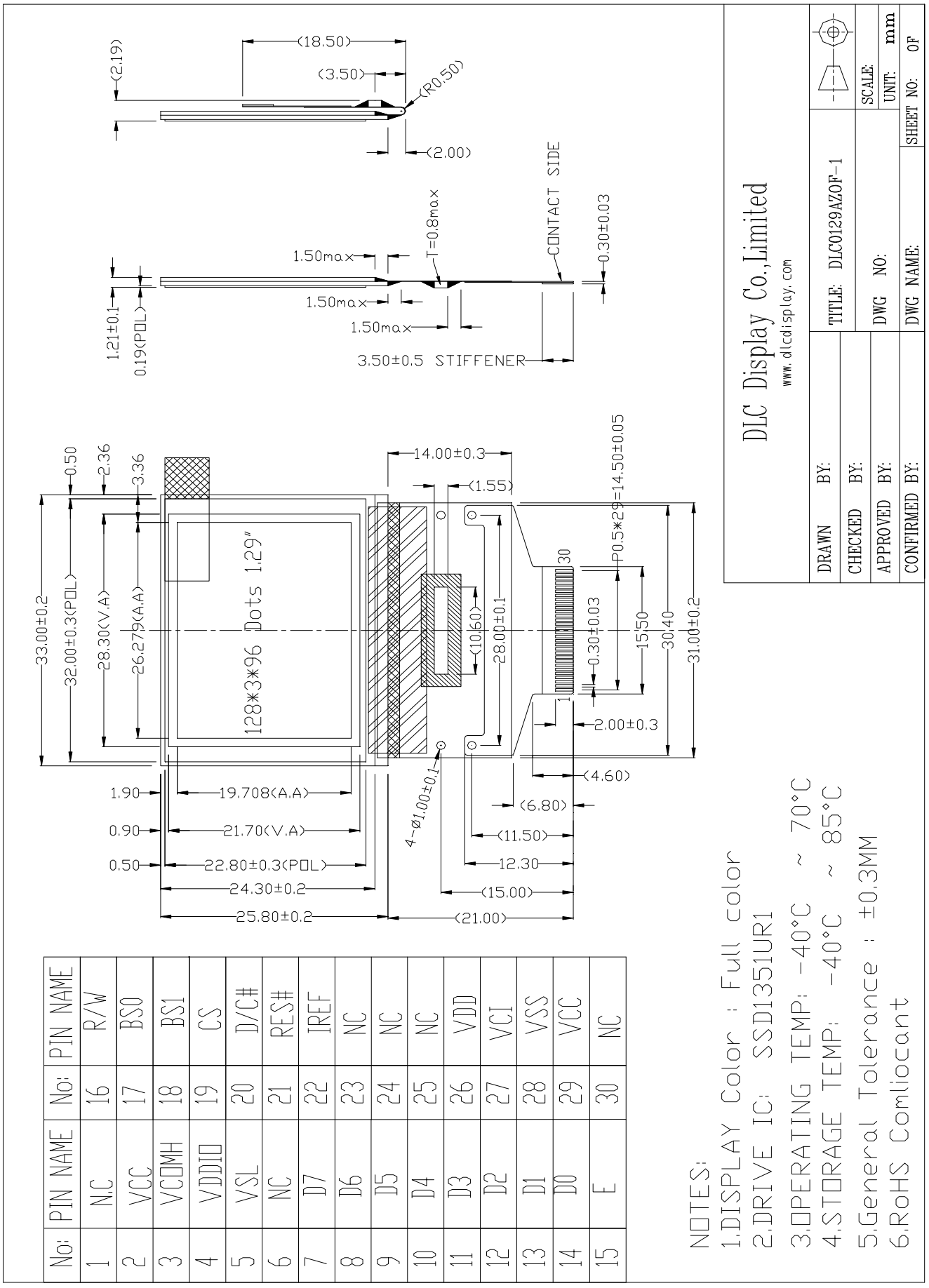
3. General Information

Item	Contents	Unit
Size	1.29	inch
Resolution	128(RGB)×96	/
Display Color	Full Color	
Interface	8 bit 8080/ 6800 parallel, SPI	
Dot Size	0.1805(W) x 0.1855 (H)	mm
Pixel pitch	0.2055(W) x 0.2055 (H)	mm
Outline Dimension	33 (W) x 25.8 (H) x 1.21 (D)	mm
Active Area	26.279 (W) x 19.708 (H)	mm
Driver IC	SSD1351UR1	
Operating Temperature	-40℃~+70℃	
Storage Temperature	-40℃~＋85℃	

4. Outline Drawing



No:	PIN NAME	No:	PIN NAME
1	N.C	16	R/W
2	VCC	17	BS0
3	VCOMH	18	BS1
4	VDDIO	19	CS
5	VSL	20	D/C#
6	NC	21	RES#
7	D7	22	IREF
8	D6	23	NC
9	D5	24	NC
10	D4	25	NC
11	D3	26	VDD
12	D2	27	VCI
13	D1	28	VSS
14	D0	29	VCC
15	E	30	NC

NOTES:
1.DISPLAY Color : Full color
2.DRIVE IC: SSD1351UR1
3.OPERATING TEMP: -40°C ~ 70°C
4.STORAGE TEMP: -40°C ~ 85°C
5.General Tolerance : ±0.3MM
6.RoHS Comliocant

5. Interface signals

Recommend connector: DDK FF14-30A-R11A

PIN NO.	PIN NAME	DESCRIPTION
1	NC	No Connection.
2	VCC	Power supply for panel driving voltage.
3	VCOMH	COM signal deselected voltage level. A capacitor should be connected between this pin and VSS.
4	VDDIO	Power supply for interface logic level.
5	VSL	This is segment voltage reference pin.
6	NC	No connection.
7--14	D7--D0	These pins are bi-directional data bus connecting to the MCU data bus.
15	E	8080: data read enable pin; 6800:Read/Write enable pin.
16	R/W#	8080: data write enable pin; 6800:Read/Write select pin.
17	BS0	Interface select pin.
18	BS1	Interface select pin.
19	CS	Chip select pin.
20	D/C#	H: Data, L: Command.
21	RES#	Hardware Reset pin (Low active).
22	IREF	A resistor should be connected between this pin and VSS.
23	NC	No Connection.
24	NC	No Connection.
25	NC	No Connection.
26	VDD	Power supply pin for core logic operation.
27	VCI	Digital voltage power supply.
28	VSS	Ground.
29	VCC	Power supply for panel driving voltage.
30	NC	No Connection.

6. Environment Conditions

6.1 Electrical Absolute max. ratings

Parameter	Symbol	MIN	MAX	Unit	Remark
Supply Voltage	VCI	-0.3	4	V	IC maximum rating
Supply Voltage	VCC	8	21	V	IC maximum rating

Note (1): Under Vcc = 15V, Ta = 25°C, 50% RH

6.2 Environment Conditions

Item	Symbol	MIN	MAX	Unit	Remark
Operating Temperature	TOPR	-40	70	℃	
Storage Temperature	TSTG	-40	85	℃	

7. Electrical Specifications

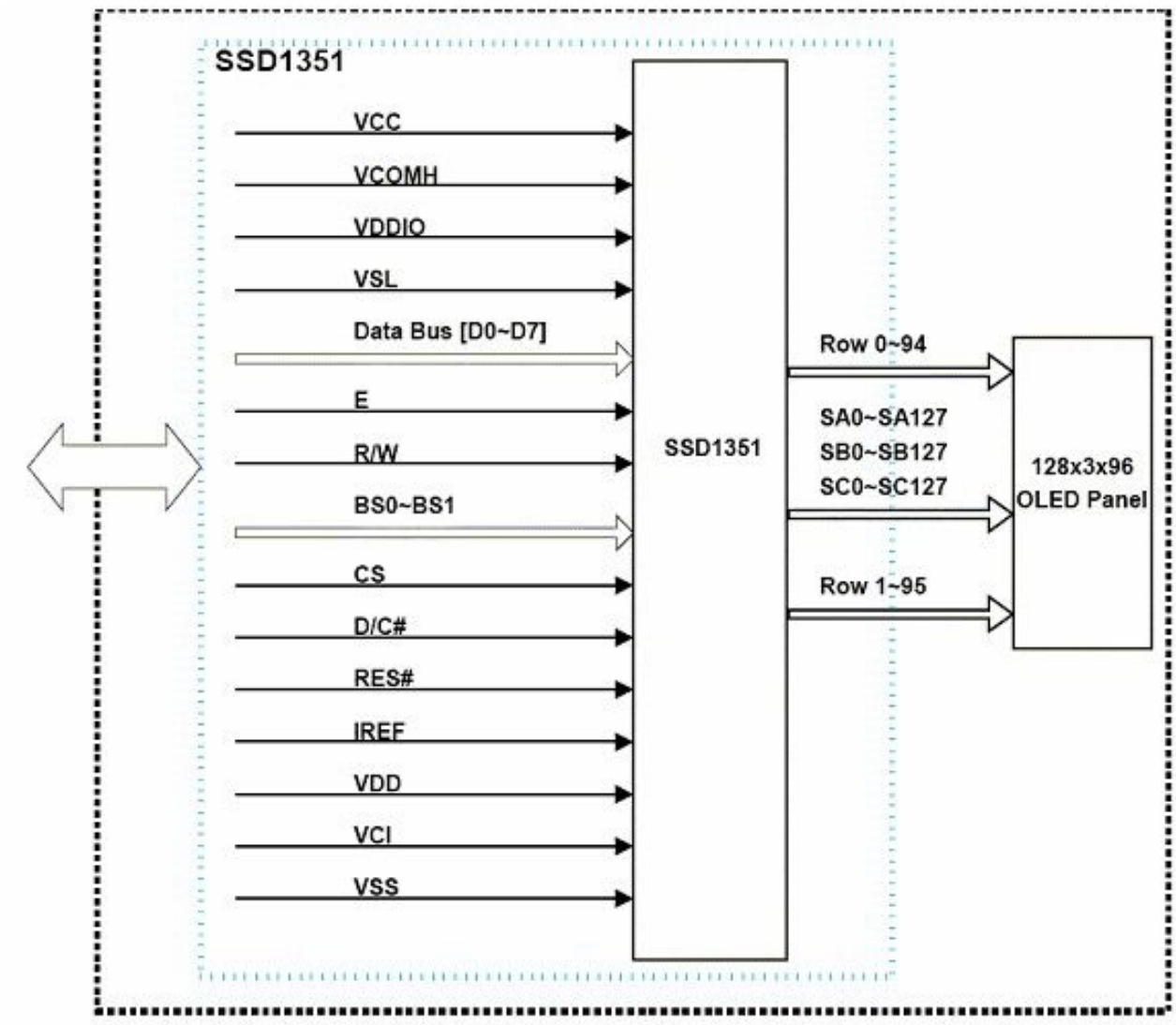
7.1 Electrical characteristics

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Digital power supply	VCI	2.4	2.8	3.5	V	
Logic I/O operating voltage	VDDIO	1.65	1.8	VCI	V	
Driver power supply (for OLED panel)	VCC	14.5	15	15.5	V	
Input Signal Voltage	VIL	0	--	0.2VDDIO	V	Iout=100uA
	VIH	0.8VDDIO	--	VDDIO	V	
output Signal Voltage	VOL	0	-	0.1 VDDIO	V	Iout=100uA
	VOH	0.9VDDIO	-	VDDIO	V	
Segment output current (VCC = 16V at IREF =12.5uA)	ISEG	--	200	--	uA	Contrast=FF
		--	100	--	uA	Contrast=7F
		--	50	--	uA	Contrast=3F
VCI = VDDIO =3.5V, VCC =16V,No panel attached, Display ON,contrast = FF	IDD	--	170	190	uA	External VDD = 2.6V,
VCI = VDDIO =, 3.5V, VCC = 16V, Display ON, No panel attached, contrast = FF	IDDIO	--	0.5	10	uA	External VDD = 2.6V
		--	0.5	10	uA	Internal VDD
VCI = VDDIO =, 3.5V, VCC = 16V, Display ON, No panel attached, contrast = FF	ICI	--	60	70	uA	External VDD = 2.6V
		--	255	280	uA	Internal VDD
VCI = VDDIO =, 3.5V, VCC = 16V, Display ON, No panel attached, contrast = FF	ICC	--	1.15	1.26	mA	External VDD = 2.6V
		--	1.15	1.26	mA	Internal VDD

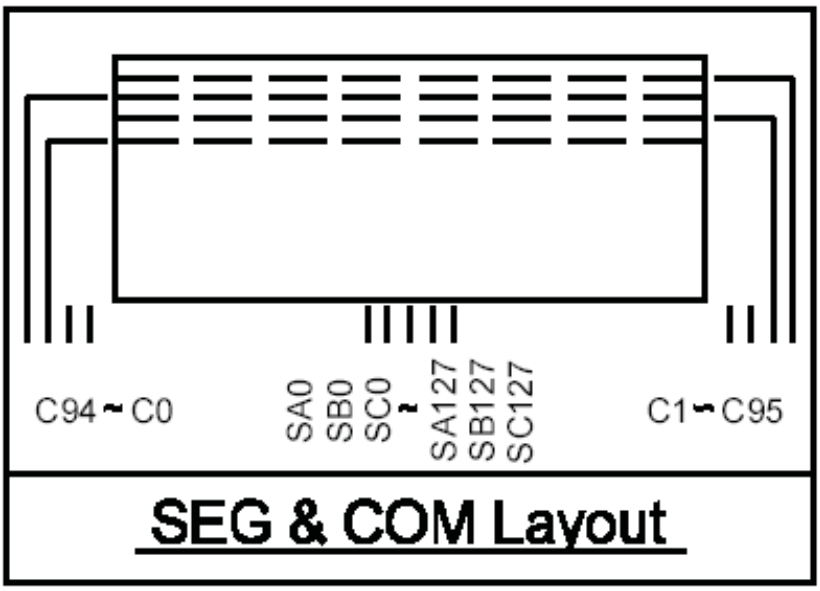
Note : The VCC input must be kept in a stable value; ripple and noise are not allowed.

7.2 Function Block Diagram

7.2.1 Function Block Diagram



7.2.2 Panel Layout Diagram



7.3 GRAPHIC DISPLAY DATA RAM ADDRESS MAP

The GDDRAM is a bit mapped static RAM holding the pattern to be displayed.The RAM size is 128 x 128 x 18bits. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. Each pixel has 18-bit data. Each sub-pixels for color A, B and C have 6 bits. The arrangement of data pixel in graphic display data RAM is shown below.

262k Color Depth Graphic Display Data RAM Structure

Segment Address	Normal	0			1			2	.....	.....	126	127			
	Remapped	127			126			125	.....	.....	1	0			
Color		A	B	C	A	B	C	A			C	A	B	C	
Data / Format		A5	B5	C5	A5	B5	C5	A5	.....	.....	C5	A5	B5	C5	
		A4	B4	C4	A4	B4	C4	A4	.....	.....	C4	A4	B4	C4	
		A3	B3	C3	A3	B3	C3	A3	.....	.....	C3	A3	B3	C3	
Common Address		A2	B2	C2	A2	B2	C2	A2	.....	.....	C2	A2	B2	C2	
		A1	B1	C1	A1	B1	C1	A1	.....	.....	C1	A1	B1	C1	
		A0	B0	C0	A0	B0	C0	A0	.....	.....	C0	A0	B0	C0	Common output
Normal	Remapped														
0	127	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM0
1	126	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM1
2	125	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM2
3	124	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM3
4	123	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM4
5	122	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM5
6	121	6	6	no of bits in this cell			6	6	.....	.....	6	6	6	6	COM6
7	120								.....	.....	6	6	6	6	COM7
:	:	:	:	:	:	:	:	:	.....	.....	:	:	:	:	:
:	:	:	:	:	:	:	:	:	.....	.....	:	:	:	:	:
:	:	:	:	:	:	:	:	:	.....	.....	:	:	:	:	:
123	4	6	6	6	6	6	6	6	.....	.....	6	6	6	6	:
124	3	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM124
125	2	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM125
126	1	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM126
127	0	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM127

SEG output	SA0	SB0	SC0	SA1	SB1	SC1	SA2	.....	.....	SC126	SA127	SB127	SC127

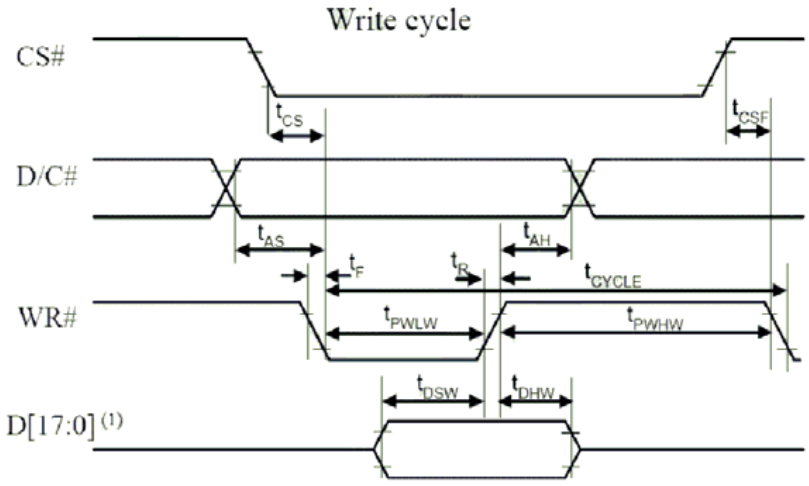
8. Command/AC Timing

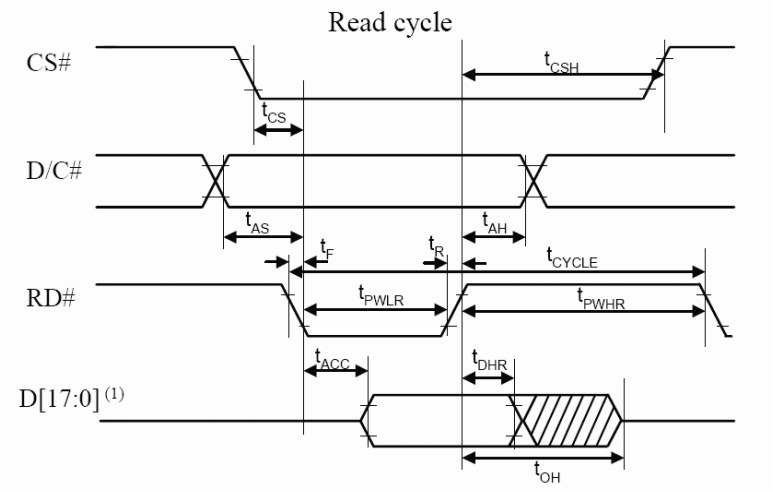
8.1 AC Electrical Characteristics

For 8080-Series MPU Parallel Interface Timing Characteristics

(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{DDIO}=1.65V, V_{CI} = 2.8V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{CYCLE}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	150	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns





Note

when 8 bit used: D[7:0] instead; when 16 bit used: [15:0] instead; when 18 bit used: D[17:0] instead.

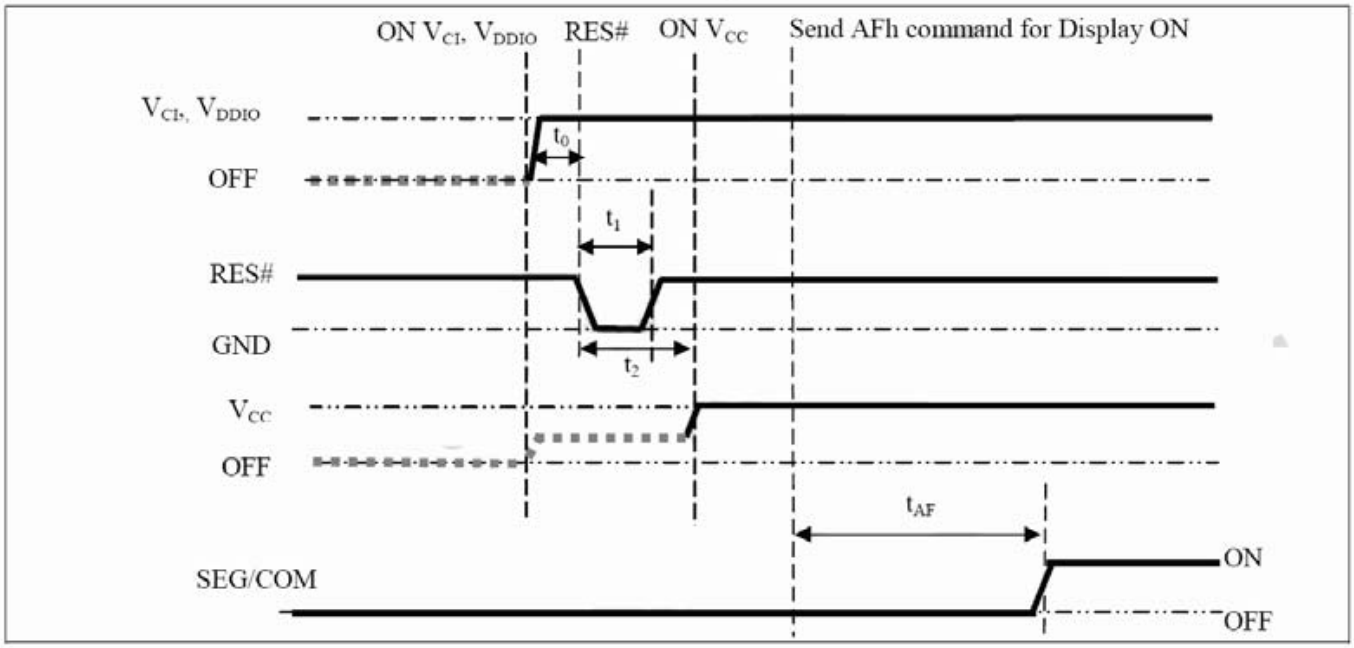
8.2 Functional Specification and Application Circuit

8.2.1 Power ON and Power OFF Sequence

The following figures illustrate the recommended power ON and power OFF sequence of SSD1351 (assume V_{CI} and V_{DDIO} are at the same voltage level and internal V_{DD} is used).

1. Power ON VCI, VDDIO.
2. After VCI, VDDIO become stable, set wait time at least 1ms (t_0) for internal VDD become stable. Then set RES# pin LOW (logic low) for at least 2us (t_1) and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 2us (t_2). Then Power ON VCC.
4. After VCC become stable, send command AFh for display ON. SEG/COM will be ON after 200ms(t_{AF}).

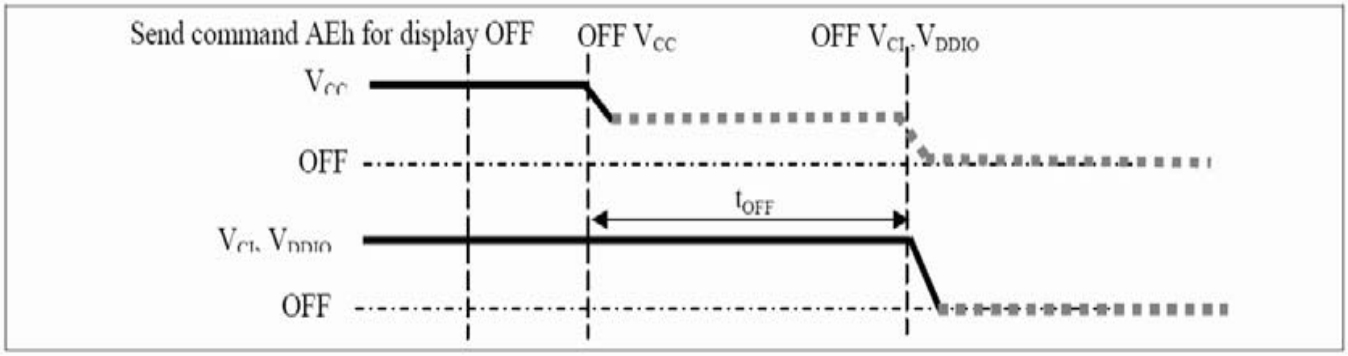
The Power ON sequence.



Power OFF sequence:

1. Send command AEh for display OFF.
2. Power OFF VCC.
3. Wait for t_{OFF}. Power OFF VCI, VDDIO.(where Minimum t_{OFF}=80ms , Typical t_{OFF}=100ms)

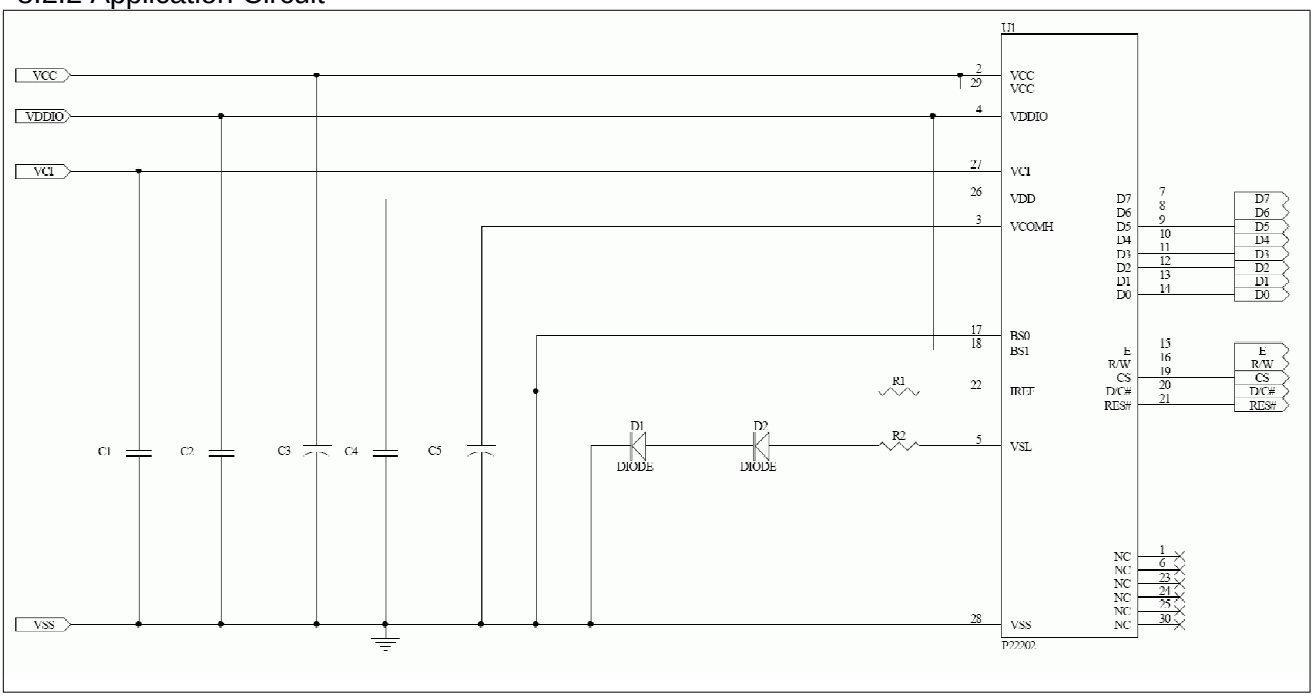
The Power OFF sequence



Note:

(1) Since an ESD protection circuit is connected between VCI, VDDIO and VCC, VCC becomes lower than VCI whenever VCI,VDDIO is ON and VCC is OFF as shown in the dotted line of VCC in above figures.
(2) VCC should be kept float (disable) when it is OFF.
(3) VCI, VDDIO should not be Power OFF before VCC Power OFF.
(4) The register values are reset after t_1.
(5) Power pins (VDD, VCC) can never be pulled to ground under any circumstance.

8.2.2 Application Circuit



Recommend components:

C1, C2, C4: 1uF/16V(0805)

C3, C5: 4.7uF/25V or 35V (Tantalum type) or VISHAY (572D475X0025A2T)

R1: 1M ohm 1%(0603)

R2: 50 ohm 1/4W

D1, D2: RB480K(ROHM)

This circuit is for 8080 8bits interface

9. Optical Specification

Ta=25℃

Item		Symbol	Condition	Min	Typ.	Max.	Unit	Remark
Contrast Ratio		CR	θ=0°	2000:1		-		Note1 Note2
View Angles		ΘT	--	160		-	Degree	Note 3
Response Time		Ton	25℃	-	10	-	us	Note1 Note3
		Toff						
Chromaticity	White	x	Brightness is on	0.24	0.28	0.32		Note5, Note1
		y		0.28	0.32	0.36		
	Red	x		0.62	0.66	0.70		
		y		0.29	0.33	0.37		
	Green	x		0.26	0.30	0.34		
		y		0.59	0.63	0.67		
	Blue	x		0.10	0.14	0.18		
		y		0.14	0.18	0.22		
Luminance		L		70	90	-	cd/m^2	Note1 Note6
Normal mode power consumption		-	All pixels ON	-	300	330	mW	
Standby mode power consumption		-	Standby mode 10% pixels on		45	75	mW	
Normal mode current		-	All pixels ON		20	22	mA	
Standby mode current		-	Standby mode 10% pixels on		3	5	mA	

Normal mode condition :

- Driving Voltage : 15V
- Contrast setting : 0x07
- Frame rate : 105Hz
- Duty setting : 1/96

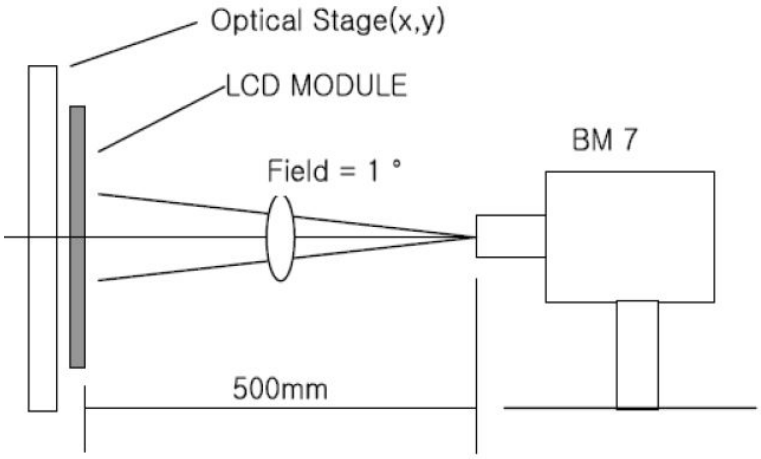
Standby mode condition :

- Driving Voltage : 15V
- Contrast setting : 0x04
- Frame rate : 105Hz
- Duty setting : 1/96

Note 1: Definition of optical measurement system.

Temperature = 25℃(±3℃)

LED back-light: ON, Environment brightness < 150 lx

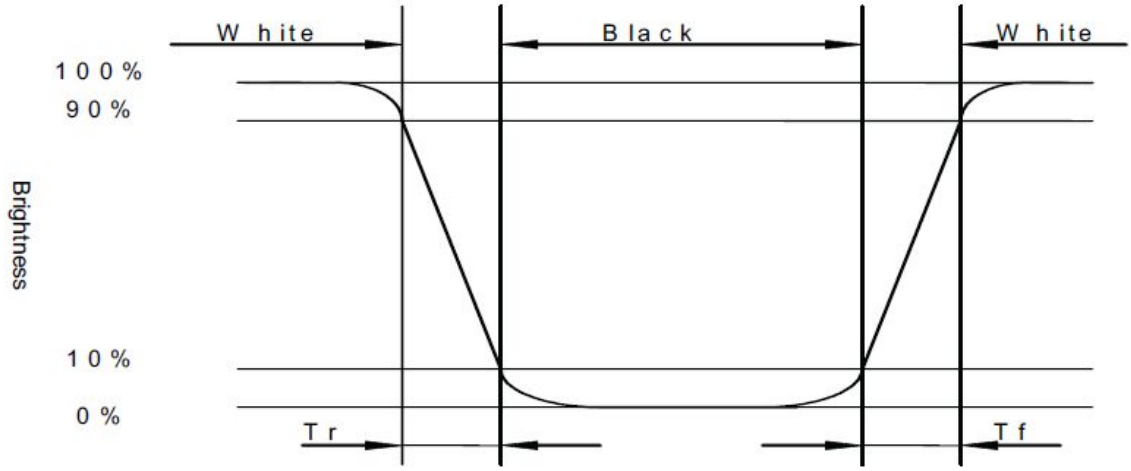


Note 2: Contrast ratio is defined as follow:

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

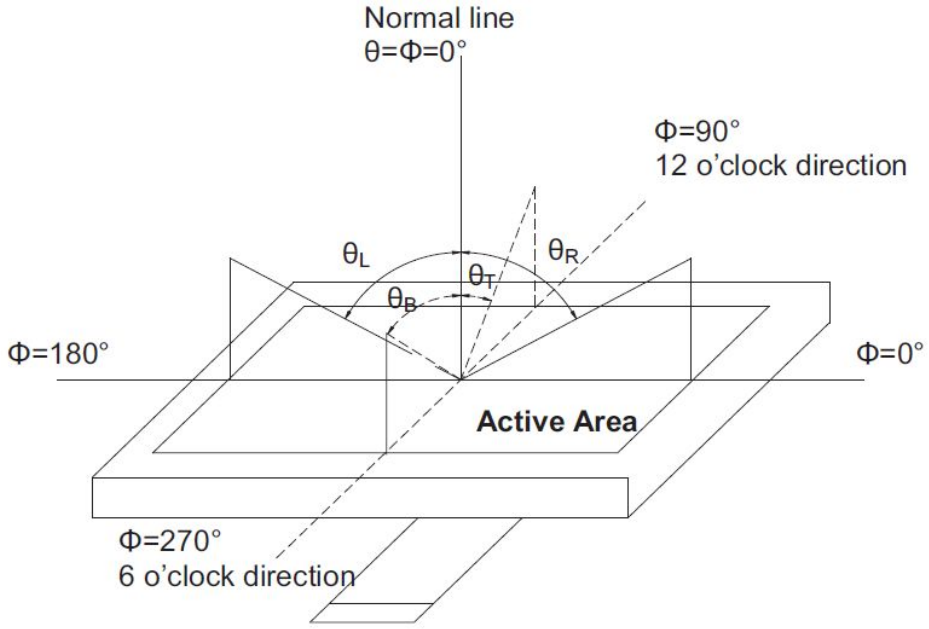
Note 3: Response time is defined as follow:

Response time is the time required for the display to transition from black to white (Rise Time, Tr) and from white to black(Decay Time, Tf).



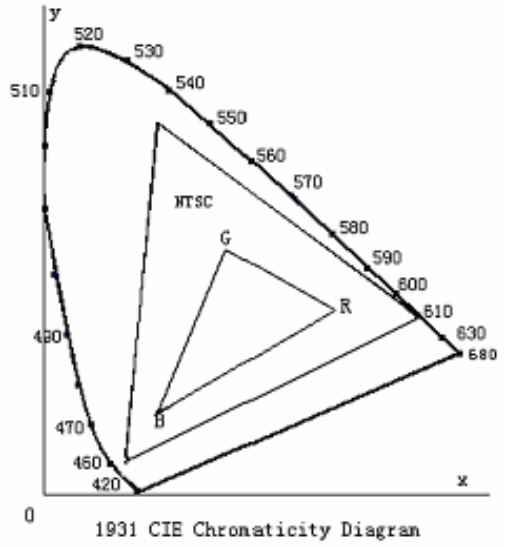
Note 4: Viewing angle range is defined as follow:

Viewing angle is measured at the center point of the LCD.



Note 5: Color chromaticity is defined as follow: (CIE1931)

Color coordinates measured at center point of LCD.



$$S = \frac{\text{area of RGB triangle}}{\text{area of NTSC triangle}} \times 100\%$$

Note 6: Luminance is defined as follow:

Luminance is defined as the brightness of all pixels "White" at the center of display area on optimum contrast.

10. Environmental / Reliability Tests

No	Test Item	Condition	Judgment criteria
1	High Temp Operation	Ts=+70℃, 120hrs	Per table in below
2	Low Temp Operation	Ta=-40℃, 120hrs	Per table in below
3	High Temp Storage	Ta=+85℃, 2400hrs	Per table in below
4	Low Temp Storage	Ta=-40℃, 120hrs	Per table in below
5	High Temp & High Humidity Storage	Ta=+65℃, 90% RH 96 hours	Per table in below (polarizer discoloration is excluded)
6	Thermal Shock (Non-operation)	-40°C ~85°C (-40°C /30min; transit /3min; 85°C /30min; transit /3min) 1cycle: 66min, 20 cycles	Per table in below
7	ESD (Operation)	Air discharge model, ±8kV, 10 times	Per table in below
8	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	Per table in below
9	Drop	Height: 120cm Sequence : 1 angle 3 edges and 6 faces Cycles: 1	Per table in below

INSPECTION	CRITERION(after test)
Appearance	No Crack on the FPC, on the OLED Panel
Alignment of OLED Panel	No Bubbles in the OLED Panel No other Defects of Alignment in Active area
Electrical current	Within device specifications Current consumption: within · 50% of initial value.
Function / Display	No Broken Circuit, No Short Circuit or No Black line No Other Defects of Display

11. Precautions for Use of OLED Modules

11.1 Safety

The liquid crystal in the OLED is poisonous. Do not put it in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and water.

11.2 Handling

A. The OLED and touch panel is made of plate glass. Do not subject the panel to mechanical shock or to excessive force on its surface.
B. Do not handle the product by holding the flexible pattern portion in order to assure the reliability
C. Transparency is an important factor for the touch panel. Please wear clear finger sacks, gloves and mask to protect the touch panel from finger print or stain and also hold the portion outside the view area when handling the touch panel.
D. Provide a space so that the panel does not come into contact with other components.
E. To protect the product from external force, put a covering lens (acrylic board or similar board) and keep an appropriate gap between them.
F. Transparent electrodes may be disconnected if the panel is used under environmental conditions where dew condensation occurs.
G. Property of semiconductor devices may be affected when they are exposed to light, possibly resulting in IC malfunctions.
H. To prevent such IC malfunctions, your design and mounting layout shall be done in the way that the IC is not exposed to light in actual use.

11.3 Static Electricity

A. Ground soldering iron tips, tools and testers when they are in operation.
B. Ground your body when handling the products.
C. Power on the OLED module before applying the voltage to the input terminals.
D. Do not apply voltage which exceeds the absolute maximum rating.
E. Store the products in an anti-electrostatic bag or container.

11.4Storage

A. Store the products in a dark place at +25℃±10℃ with low humidity (40% RH to 60% RH). Don't expose to sunlight or fluorescent light.
B. Storage in a clean environment, free from dust, active gas, and solvent.

11.5 Cleaning

A. Do not wipe the touch panel with dry cloth, as it may cause scratch.
B. Wipe off the stain on the product by using soft cloth moistened with ethanol. Do not allow ethanol to get in between the upper film and the bottom glass. It may cause peeling issue or defective operation. Do not use any organic solvent or detergent other than ethanol.

11.6 Cautions for installing and assembling

Bezel edge must be positioned in the area between the Active area and View area. The bezel may press the touch screen and cause activation if the edge touches the active area. A gap of approximately 0.5mm is needed between the bezel and the top electrode. It may cause unexpected activation if the gap is too narrow. There is a tolerance of 0.2 to 0.3mm for the outside dimensions of the touch panel and tail. A gap must be made to absorb the tolerance in the case and connector.