# DLC Display Co., Limited

# 德爾西顯示器有限公司

MODEL No: DLC0112AZOG

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# Record of Revision

| Date | Revision No. | Summary |
|---|---|---|
| 2014-03-31 | 1.0 | Rev 1.0 was issued |
| | | |

## 1. Scope

This data sheet is to introduce the specification of DLC0112AZOG, passive matrix OLED module. It is composed of an OLED panel, driver ICs and FPC. The1.12″ display area contains 96 x 96 pixels.

## 2. Application

Digital equipments which need display, instrumentation, remote control, electronic product.
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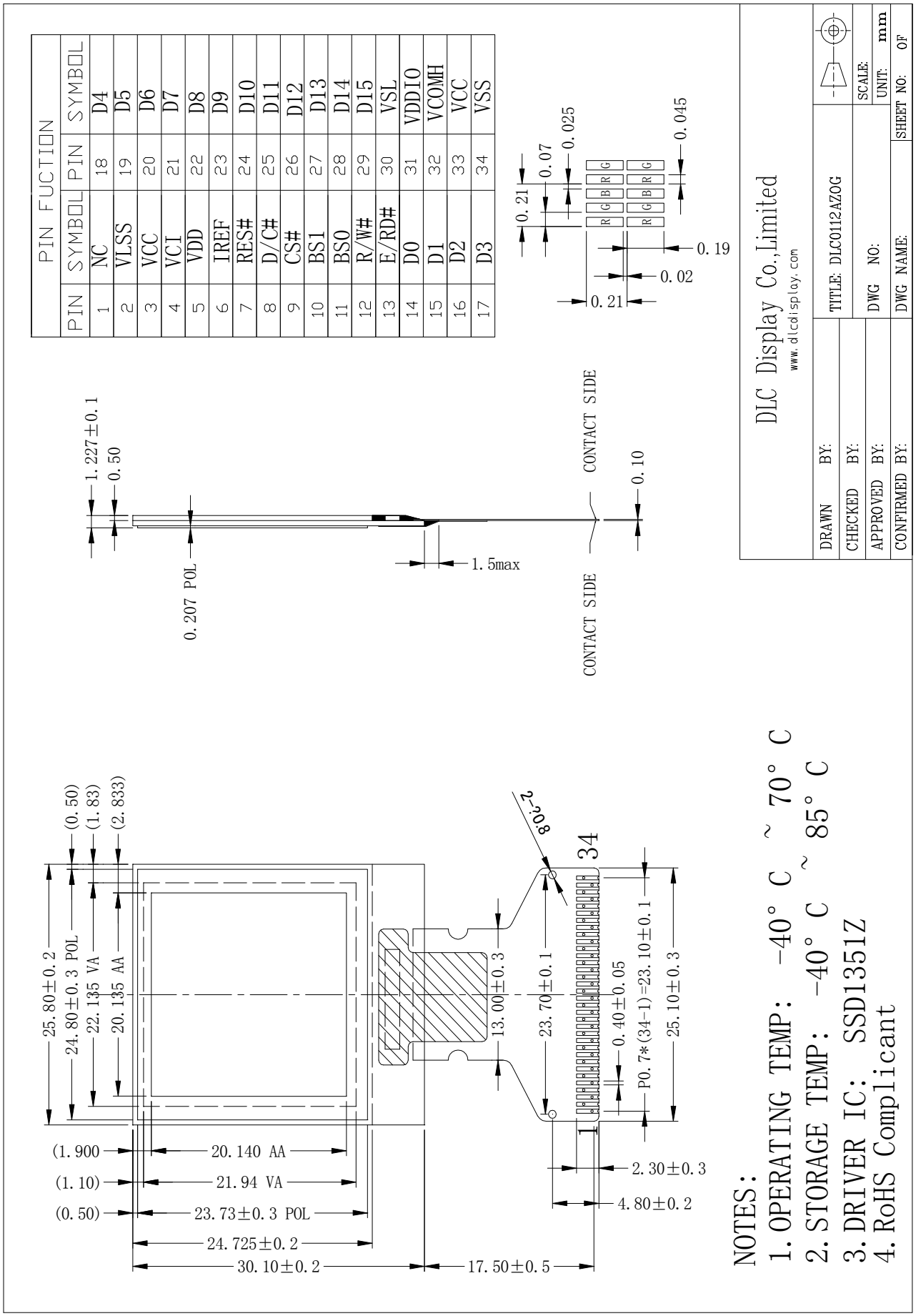
## 3. General Information

| Item | Contents | Unit |
|---|---|---|
| Size | 1.12 | inch |
| Resolution | 96(RGB)×96 | / |
| Display Color | Full Color | |
| Interface | 8/16-bit 8080 parallel, SPI | |
| Dot Size | 0.045(W) x 0.19 (H) | mm |
| Pixel pitch | 0.07(W) x 0.21 (H) | mm |
| Outline Dimension | 25.8 (W) x 30.1 (H) x 1.227(D) | mm |
| Active Area | 20.135 (W) x 20.14 (H) | mm |
| Driver IC | SSD1351Z | |
| Drive Duty | 1/96 Duty | / |
| Weight | 1.89 | g |
| Operating Temperature | -40℃~+70℃ | |
| Storage Temperature | -40℃~＋85℃ | |

## 4. Outline Drawing



## 5. Interface signals

| PIN NO. | PIN NAME | DESCRIPTION |
|---|---|---|
| 1 | NC | No Connection. |
| 2 | VLSS | Analog system ground pin |
| 3 | VCC | Power supply for panel driving voltage. |
| 4 | VCI | Low voltage power supply VCI must always be equal to or higher than VDD and VDDIO. |
| 5 | VDD | Power supply pin for core logic operation. |
| 6 | IREF | A resistor should be connected between this pin and VSS. |
| 7 | RES# | Hardware Reset pin (Low active). |
| 8 | D/C# | This pin is Data/Command control pin connecting to the MCU. |
| 9 | CS# | This pin is the chip select input connecting to the MCU. |
| 10 | BS1 | Interface select pin. |
| 11 | BS0 | Interface select pin. |
| 12 | R/W# | This pin is read / write control input pin connecting to the MCU interface. |
| 13 | E/RD# | This pin is MCU interface input.<br>When 8080 interface mode is selected, this pin receives the Read (RD#) signal.<br>Read operation is initiated when this pin is pulled LOW and the chip is selected.<br>When serial interface is selected, this pin E(RD#) must be connected to VSS. |
| 14--29 | D0--D15 | These pins are bi-directional data bus connecting to the MCU data bus.<br>Unused pins are recommended to tie LOW. (Except for D2 pin in SPI mode) |
| 30 | VSL | This is segment voltage reference pin. External VSL is set as default. This pin has to connect with resistor and diode to ground. (Details depend on application) |
| 31 | VDDIO | Power supply for interface logic level. |
| 32 | VCOMH | COM signal deselected voltage level.<br>A capacitor should be connected between this pin and VSS. |
| 33 | VCC | Power supply for panel driving voltage. |
| 34 | VSS | Ground |

# 6. Environment Conditions

## 6.1 Electrical Absolute max. ratings

| Parameter | Symbol | MIN | MAX | Unit | Remark |
|---|---|---|---|---|---|
| Supply Voltage | VCI | -0.3 | 4 | V | IC maximum rating |
| Supply Voltage | VCC | 10 | 21 | V | IC maximum rating |

Note (1): Under Vcc = 16.5V, Ta = 25°C, 50% RH

## 6.2 Environment Conditions

| Item | Symbol | MIN | MAX | Unit | Remark |
|---|---|---|---|---|---|
| Operating Temperature | TOPR | -40 | 70 | ℃ | |
| Storage Temperature | TSTG | -40 | 85 | ℃ | |

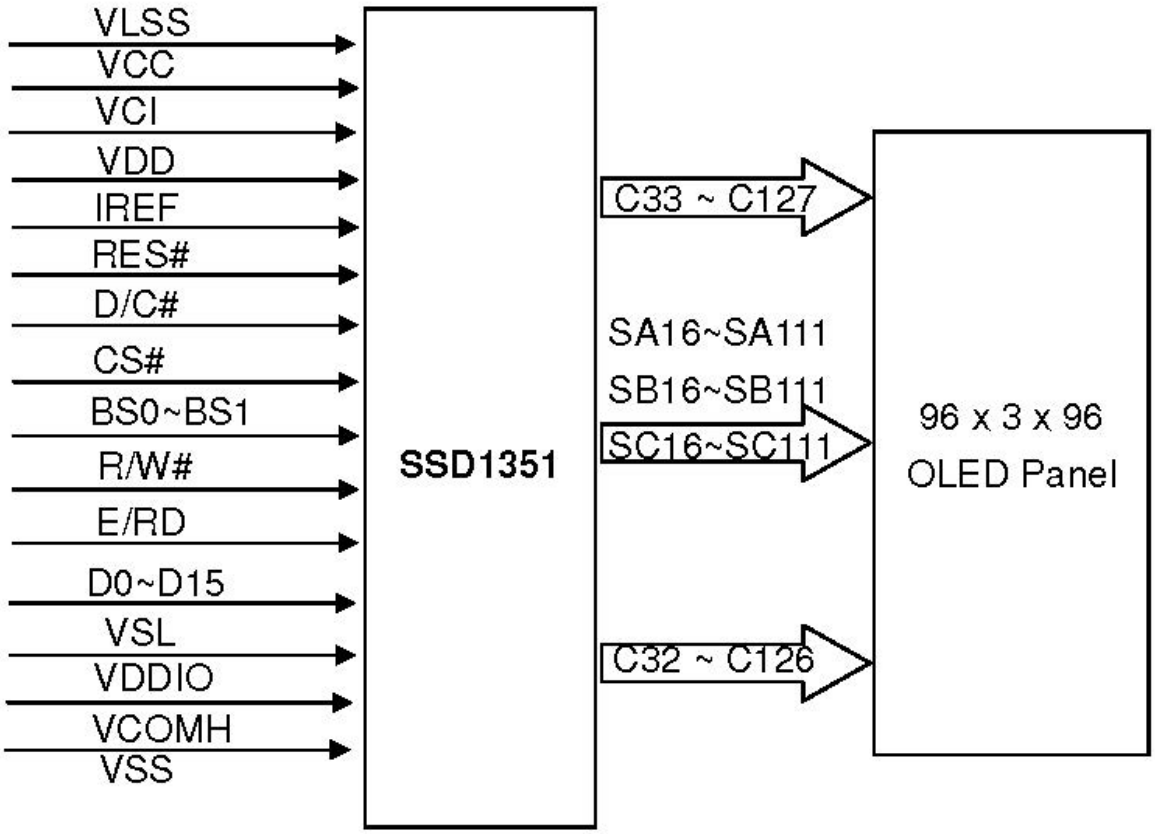
# 7. Electrical Specifications

## 7.1 Electrical characteristics

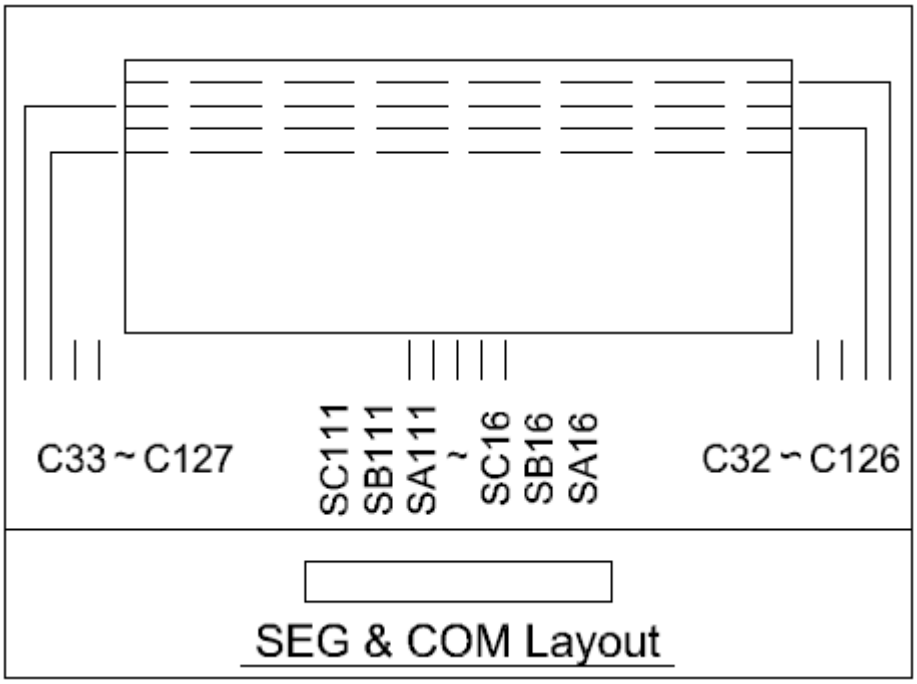
| Item | Symbol | MIN | TYP | MAX | Unit | Remark |
|---|---|---|---|---|---|---|
| Analog power supply (for OLED panel) | $V_{CC}$ | 14.5 | 15 | 15.5 | V | |
| Digital power supply | $V_{CI}$ | 2.4 | 2.8 | 3.5 | V | |
| Power Supply for I/O pins | $V_{DDIO}$ | 1.65 | 1.8 | VCI | V | |
| $V_{CI}$ = $V_{DDIO}$ =3.5V, $V_{CC}$ = 16V, External $V_{DD}$ = 2.6V, Display ON,No panel attached, contrast = FF | $I_{DD}$ | - | 170 | 190 | uA | |
| $V_{CI}$ = $V_{DDIO}$ =, 3.5V, $V_{CC}$ = 16V, Display ON, No panel attached, contrast = FF | $I_{DDIO}$ | - | 0.5 | 10 | uA | External $V_{DD}$ = 2.6V |
| | | - | 0.5 | 10 | uA | Internal $V_{DD}$ |
| $V_{CI}$ = $V_{DDIO}$ =, 3.5V, $V_{CC}$ = 16V, Display ON, No panel attached, contrast = FF | $I_{CI}$ | - | 60 | 70 | uA | External $V_{DD}$ = 2.6V |
| | | - | 255 | 280 | uA | Internal $V_{DD}$ |
| $V_{CI}$ = $V_{DDIO}$ =, 3.5V, $V_{CC}$ = 16V, Display ON, No panel attached, contrast = FF | $I_{CC}$ | - | 1.15 | 1.26 | mA | External $V_{DD}$ = 2.6V |
| | | - | 1.15 | 1.26 | mA | Internal $V_{DD}$ |
| High logic Input Voltage | $V_{IH}$ | 0.8×$V_{DDIO}$ | - | $V_{DDIO}$ | V | |
| Low logic Input Voltage | $V_{IL}$ | 0 | - | 0.2×$V_{DDIO}$ | V | |
| High logic Output Voltage | $V_{OH}$ | 0.9×$V_{DDIO}$ | - | $V_{DDIO}$ | V | |
| Low logic Output Voltage | $V_{OL}$ | 0 | - | 0.1×$V_{DDIO}$ | V | |
| Segment Output Current Setting $V_{CC}$ = 16V at IREF = 12.5uA | $I_{SEG}$ | - | 200 | - | uA | Contrast=FF |
| | | - | 100 | - | uA | Contrast=7F |
| | | - | 50 | - | uA | Contrast=3F |

## 7.2 Function Block Diagram

### 7.2.1 Function Block Diagram




### 7.2.2 Panel Layout Diagram



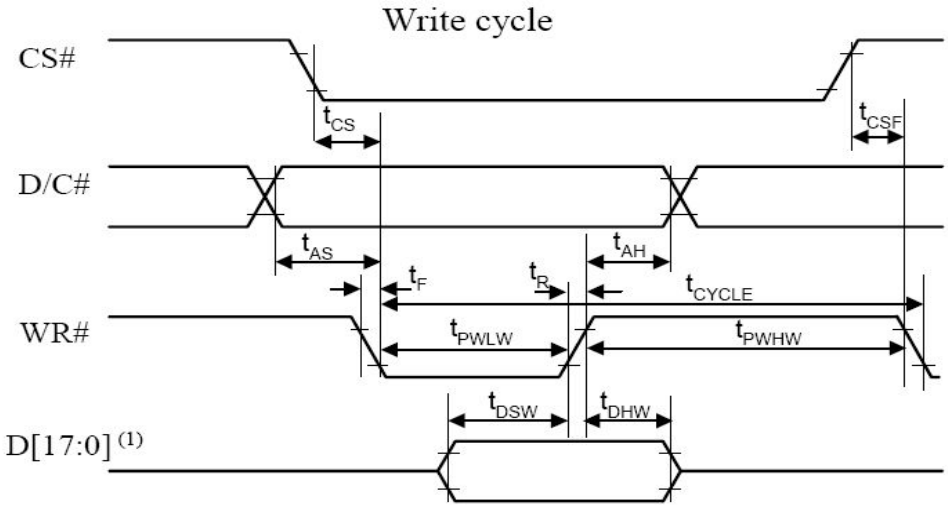
# 8. Command/AC Timing

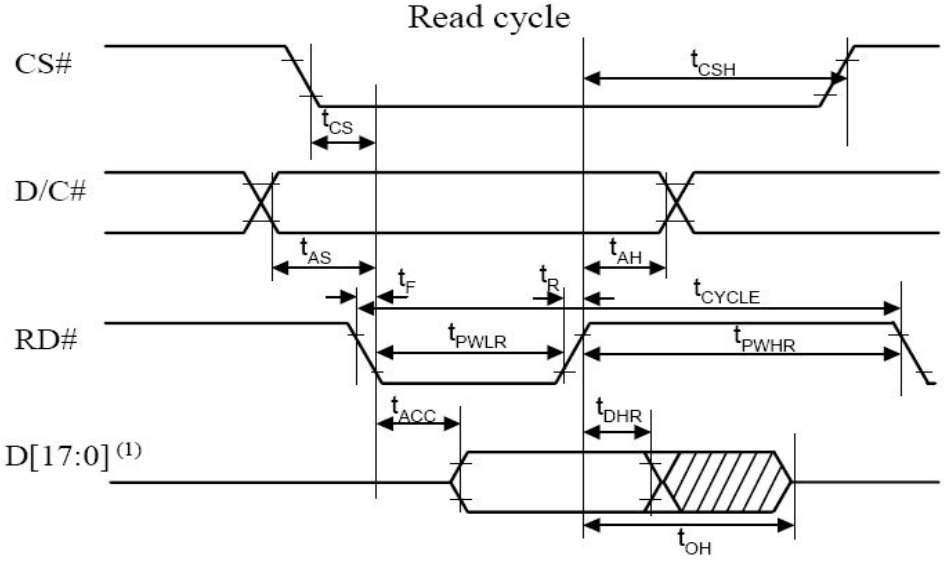
## 8.1 AC Electrical Characteristics

For 8080-Series MPU Parallel Interface Timing Characteristics

($V_{DD}$ - $V_{SS}$ = 2.4 to 2.6V, $V_{DDIO}$=1.65V, $V_{CI}$ = 2.8V, $T_A$ = 25°C)

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{CYCLE}$ | Clock Cycle Time | 300 | - | - | ns |
| $t_{AS}$ | Address Setup Time | 10 | - | - | ns |
| $t_{AH}$ | Address Hold Time | 0 | - | - | ns |
| $t_{DSW}$ | Write Data Setup Time | 40 | - | - | ns |
| $t_{DHW}$ | Write Data Hold Time | 7 | - | - | ns |
| $t_{DHR}$ | Read Data Hold Time | 20 | - | - | ns |
| $t_{OH}$ | Output Disable Time | - | - | 70 | ns |
| $t_{ACC}$ | Access Time | - | - | 140 | ns |
| $t_{PWLR}$ | Read Low Time | 150 | - | - | ns |
| $t_{PWLW}$ | Write Low Time | 60 | - | - | ns |
| $t_{PWHR}$ | Read High Time | 60 | - | - | ns |
| $t_{PWHW}$ | Write High Time | 60 | - | - | ns |
| $t_R$ | Rise Time | - | - | 15 | ns |
| $t_F$ | Fall Time | - | - | 15 | ns |
| $t_{CS}$ | Chip select setup time | 0 | - | - | ns |
| $t_{CSH}$ | Chip select hold time to read signal | 0 | - | - | ns |
| $t_{CSF}$ | Chip select hold time | 20 | - | - | ns |



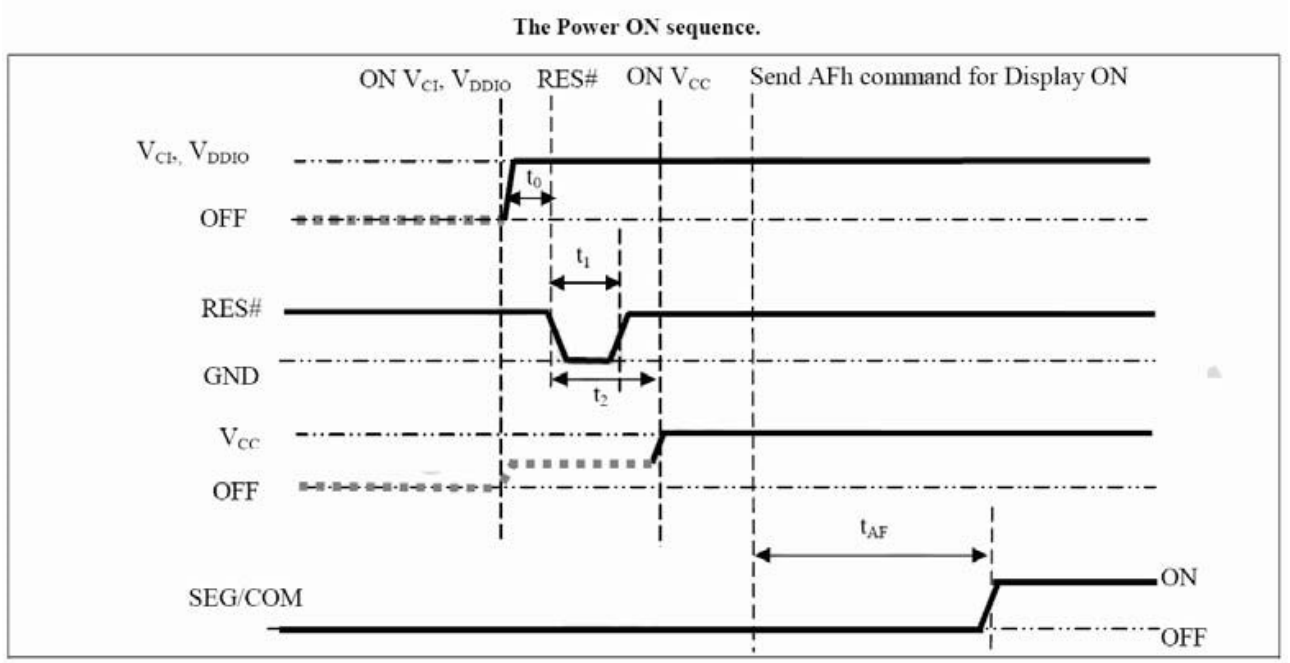
## 8.2 Functional Specification and Application Circuit

### 8.2.1 Power ON and Power OFF Sequence

The following figures illustrate the recommended power ON and power OFF sequence of SSD1351 (assume VCI and VDDIO are at the same voltage level and internal VDD is used).

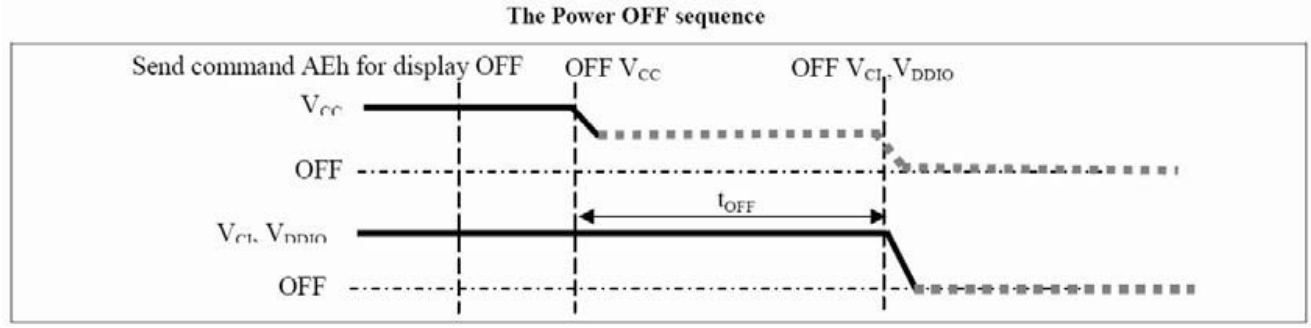
Power ON Sequence:

1. Power ON VCI, VDDIO.
2. After VCI, VDDIO become stable, set wait time at least 1ms (t0) for internal VDD become stable. Then set RES# pin LOW (logic low) for at least 2us (t1) (4) and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 2us (t2). Then Power ON VCC.
4. After VCC become stable, send command AFh for display ON. SEG/COM will be ON after 200ms(tAF).




Power OFF sequence:

1. Send command AEh for display OFF.
2. Power OFF VCC.
3. Wait for tOFF. Power OFF VCI, VDDIO.(where Minimum tOFF=80ms , Typical tOFF=100ms)




Note:

(1) Since an ESD protection circuit is connected between VCI, VDDIO and VCC, VCC becomes lower than VCI whenever VCI,VDDIO is ON and VCC is OFF as shown in the dotted line of VCC in above figures.

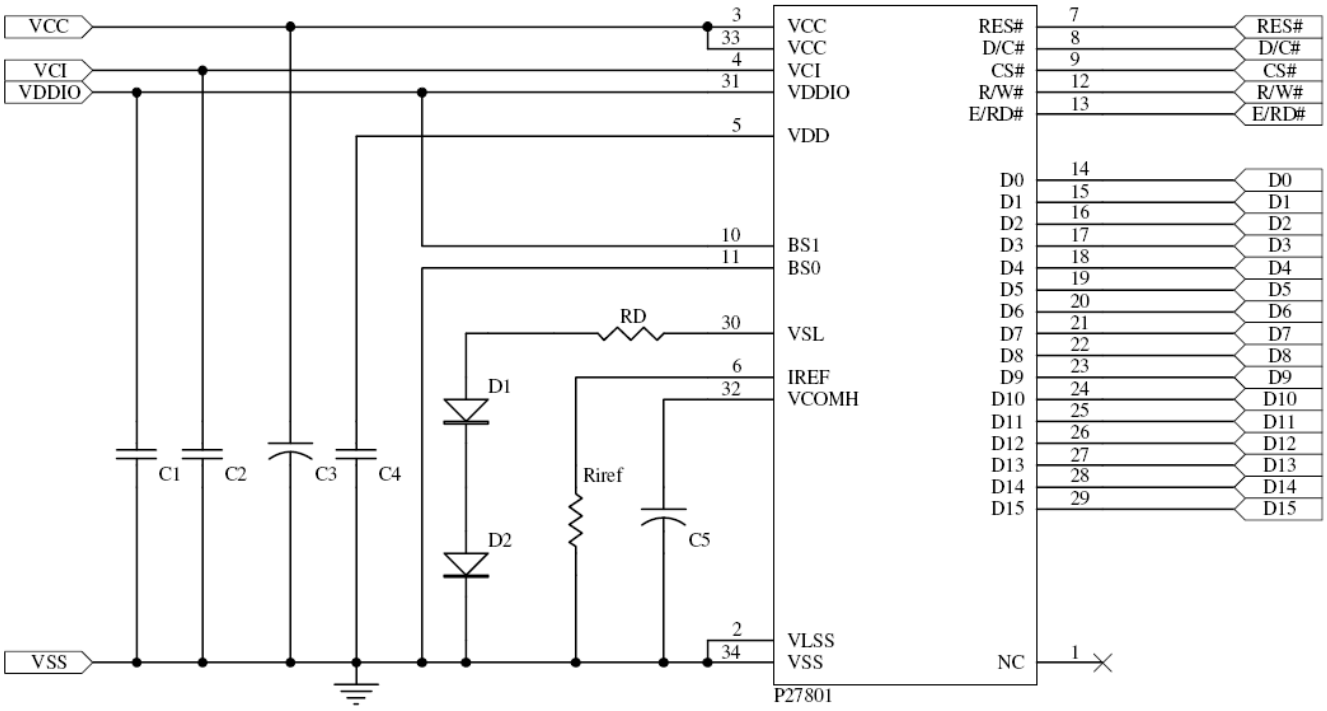
(2) VCC should be kept float (disable) when it is OFF.

(3) VCI, VDDIO should not be Power OFF before VCC Power OFF.

(4) The register values are reset after t1.

(5) Power pins (VDD, VCC) can never be pulled to ground under any circumstance.

8.2.2 Application Circuit




Recommend components:

C1、C2、C4： 1uF/16V(0805)

C3、C5：4.7uF/35V (Tantalum type) or VISHAY (572D475X0025A2T)

Riref：1M ohm 1% (0603)

RD：50 ohm 1/4W

D1、D2：RB480K (ROHM)

This circuit is designed for 16bit 8080 interface.

## 9. Optical Specification

Ta=25℃

| Item | | Symbol | Condition | Min | Typ. | Max. | Unit | Remark |
|---|---|---|---|---|---|---|---|---|
| Contrast Ratio | | CR | θ=0° | 2000:1 | | - | | Note1 Note2 |
| View Angles | | ΘT | -- | 160 | | - | Degree | Note 3 |
| Response Time | | Ton | 25℃ | - | 10 | - | us | Note1 Note3 |
| | | Toff | | | | | | |
| Chromaticity | White | x | Brightness is on | 0.24 | 0.28 | 0.32 | | Note5, Note1 |
| | | y | | 0.28 | 0.32 | 0.36 | | |
| | Red | x | | 0.62 | 0.66 | 0.70 | | |
| | | y | | 0.29 | 0.32 | 0.37 | | |
| | Green | x | | 0.26 | 0.30 | 0.34 | | |
| | | y | | 0.59 | 0.63 | 0.67 | | |
| | Blue | x | | 0.10 | 0.14 | 0.18 | | |
| | | y | | 0.14 | 0.18 | 0.22 | | |
| Normal mode Luminance | | L | Display Average | 60 | 80 | - | $cd/m^2$ | Note1 Note6 |
| Standby mode Luminance | | L | | | 20 | - | $cd/m^2$ | |

Note:

(1) Normal mode condition :

- Driving Voltage : 15V
- Master contrast setting : 0x0c
- Blue contrast setting : 0x6b
- Green contrast setting : 0x3c
- Red contrast setting : 0x42
- Frame rate : 105Hz
- Duty setting : 1/96

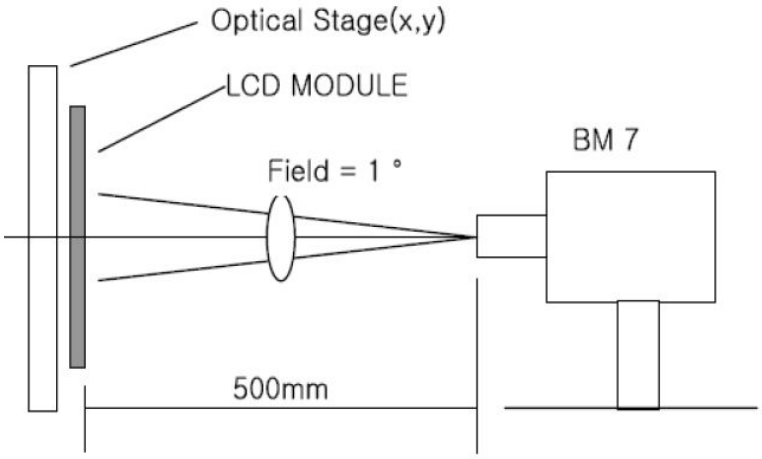
(2) Standby mode condition :

- Driving Voltage : 15V
- Master contrast setting : 0x04
- Blue contrast setting : 0x61
- Green contrast setting : 0x38
- Red contrast setting : 0x3b
- Frame rate : 105Hz
- Duty setting : 1/96

Note 1: Definition of optical measurement system.

Temperature = 25℃(±3℃)

LED back-light: ON, Environment brightness < 150 lx

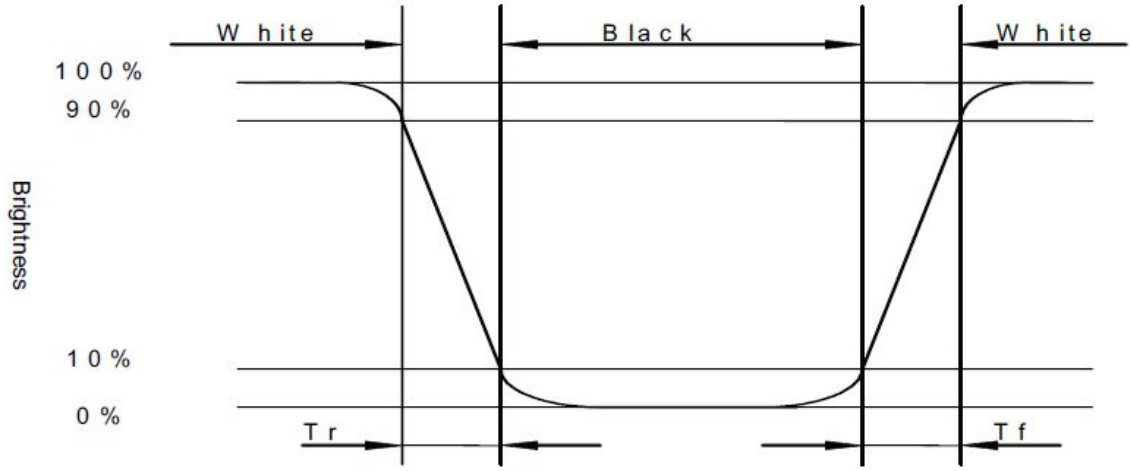



Note 2: Contrast ratio is defined as follow:

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

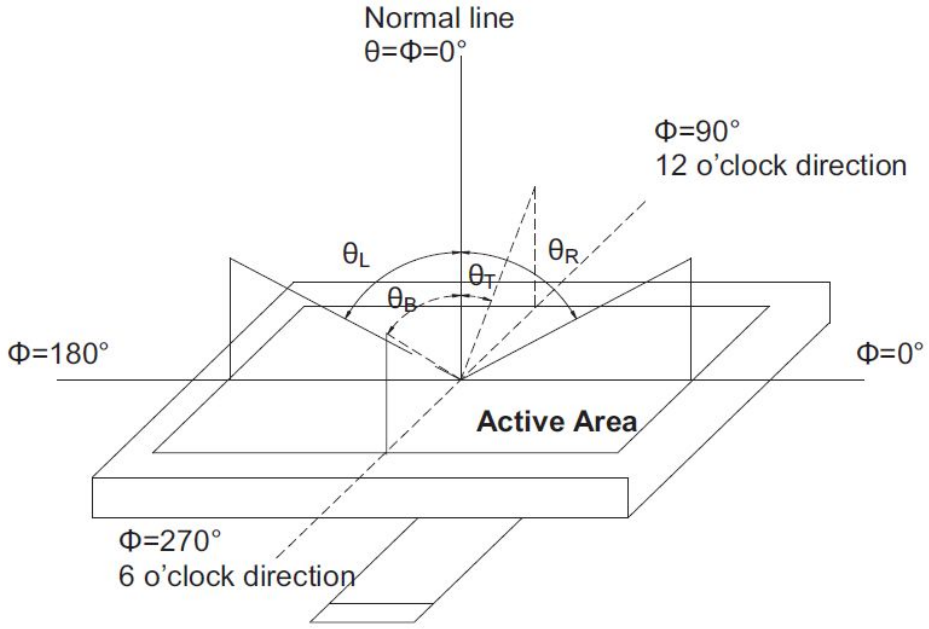
Note 3: Response time is defined as follow:

Response time is the time required for the display to transition from black to white (Rise Time, Tr) and from white to black(Decay Time, Tf).



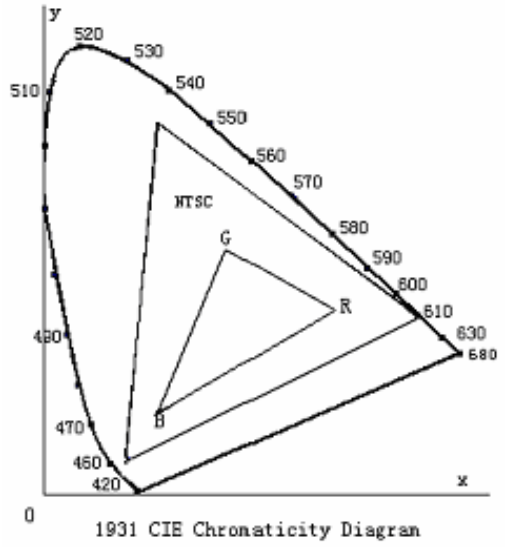
Note 4: Viewing angle range is defined as follow:

Viewing angle is measured at the center point of the LCD.




Note 5: Color chromaticity is defined as follow: (CIE1931)

Color coordinates measured at center point of LCD.




1931 CIE Chromaticity Diagram

$$S = \frac{\text{area of RGB triangle}}{\text{area of NTSC triangle}} \times 100\%$$

Note 6: Luminance is defined as follow:

Luminance is defined as the brightness of all pixels “White” at the center of display area on optimum contrast.

## 10. Environmental / Reliability Tests

| No | Test Item | Condition | Judgment criteria |
|---|---|---|---|
| 1 | High Temp Operation | Ts=+70℃, 120hrs | Per table in below |
| 2 | Low Temp Operation | Ta=-40℃, 120hrs | Per table in below |
| 3 | High Temp Storage | Ta=+85℃, 120hrs | Per table in below |
| 4 | Low Temp Storage | Ta=-40℃, 120hrs | Per table in below |
| 5 | High Temp & High Humidity Storage | Ta=+65℃, 90% RH<br>96 hours | Per table in below<br>(polarizer discoloration is excluded) |
| 6 | Thermal Shock (Non-operation) | -40°C ~85°C (-40°C /30min; transit /3min; 85°C /30min; transit /3min) 1cycle: 66min, 20 cycles | Per table in below |
| 7 | ESD (Operation) | Air discharge model, ±8kV, 10 times | Per table in below |
| 8 | Vibration | Frequency : 5~50HZ, 0.5G<br>Scan rate : 1 oct/min<br>Time : 2 hrs/axis<br>Test axis : X, Y, Z | Per table in below |
| 9 | Drop | Height: 120cm<br>Sequence : 1 angleǵ 3 edges and 6 faces | Per table in below |
| 10 | Package Drop Test | Height:80 cm,<br>1 corner, 3 edges, 6 surfaces | Per table in below |

| INSPECTION | CRITERION(after test) |
|---|---|
| Appearance | No Crack on the FPC, on the OLED Panel |
| Alignment of OLED Panel | No Bubbles in the OLED Panel<br>No other Defects of Alignment in Active area |
| Electrical current | Within device specifications<br>Current consumption: within · 50% of initial value. |
| Function / Display | No Broken Circuit, No Short Circuit or No Black line<br>No Other Defects of Display |

# 11. Precautions for Use of OLED Modules

## 11.1 Safety

The liquid crystal in the OLED is poisonous. Do not put it in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and water.

## 11.2 Handling

A. The OLED and touch panel is made of plate glass. Do not subject the panel to mechanical shock or to excessive force on its surface.
B. Do not handle the product by holding the flexible pattern portion in order to assure the reliability
C. Transparency is an important factor for the touch panel. Please wear clear finger sacks, gloves and mask to protect the touch panel from finger print or stain and also hold the portion outside the view area when handling the touch panel.
D. Provide a space so that the panel does not come into contact with other components.
E. To protect the product from external force, put a covering lens (acrylic board or similar board) and keep an appropriate gap between them.
F. Transparent electrodes may be disconnected if the panel is used under environmental conditions where dew condensation occurs.
G. Property of semiconductor devices may be affected when they are exposed to light, possibly resulting in IC malfunctions.
H. To prevent such IC malfunctions, your design and mounting layout shall be done in the way that the IC is not exposed to light in actual use.

## 11.3 Static Electricity

A. Ground soldering iron tips, tools and testers when they are in operation.
B. Ground your body when handling the products.
C. Power on the OLED module before applying the voltage to the input terminals.
D. Do not apply voltage which exceeds the absolute maximum rating.
E. Store the products in an anti-electrostatic bag or container.

## 11.4Storage

A. Store the products in a dark place at +25℃±10℃ with low humidity (40% RH to 60% RH). Don't expose to sunlight or fluorescent light.
B. Storage in a clean environment, free from dust, active gas, and solvent.

## 11.5 Cleaning

A. Do not wipe the touch panel with dry cloth, as it may cause scratch.
B. Wipe off the stain on the product by using soft cloth moistened with ethanol. Do not allow ethanol to get in between the upper film and the bottom glass. It may cause peeling issue or defective operation. Do not use any organic solvent or detergent other than ethanol.

## 11.6 Cautions for installing and assembling

Bezel edge must be positioned in the area between the Active area and View area. The bezel may press the touch screen and cause activation if the edge touches the active area. A gap of approximately 0.5mm is needed between the bezel and the top electrode. It may cause unexpected activation if the gap is too narrow. There is a tolerance of 0.2 to 0.3mm for the outside dimensions of the touch panel and tail. A gap must be made to absorb the tolerance in the case and connector.